

USER MANUAL



VERY HIGH DENSITY VERSATILE MULTIPLEXER MODULE (MODEL No. 40-612)



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<http://www.pickeringtest.com>

Pickering Interfaces Headquarters

Stephenson Road Clacton-on-Sea CO15 4NL United Kingdom

Tel: +44 (0)1255-687900

Fax: +44 (0)1255-425349

E-Mail: sales@pickeringtest.com

Pickering Interfaces Inc.
2900 Northwest Vine Street
Grants Pass
Oregon 97526
USA

Tel: +1 541 471 0700

Fax: +1 541 471 8828

E-Mail: ussales@pickeringtest.com

Pickering Interfaces GmbH
Johann-Karg-Straße 30
D-85540
Haar-Salmdorf
Germany

Tel: +49 89 125 953 160

Fax: +49 89 125 953 189

E-Mail: desales@pickeringtest.com

Pickering Interfaces AB
Karl Nordströmsväg 31
432 53
Varberg
Sweden

Tel: +46 340-69 06 69

Fax: +46 340-69 06 68

E-Mail: ndsales@pickeringtest.com

Pickering Interfaces Inc.
(East Coast Regional Office)
12 Alfred Street Suite 300-3
Woburn Massachusetts 01801
USA

Tel: +1 781 897 1710

Fax: +1 781 897 1701

E-mail: useastsales@pickeringtest.com

Pickering Interfaces s.r.o.
Smetanova 525
Třinec
739 61
Czech Republic

Tel: +42 0558 339 168

Fax: +42 0558 340 888

E-mail: cesales@pickeringtest.com

Pickering Interfaces SARL
6 Rue De La Mare Blanche
77186 Noisiel
Marne Le Vallee
France

Tel +33 1 60 53 55 50

Fax +33 1 60 53 55 99

email frsales@pickeringtest.com

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CONTENTS

Copyright Statement	ii
Technical Support and Warranty.....	iii
Contents (this page).....	v
Section 1	
Introduction.....	1.1
Section 2	
Technical Specification.....	2.1
Section 3	
Installation.....	3.1
Section 4	
Programming	4.1
Programming Options for PXI Cards.....	4.1
Card Architecture	4.2
Soft Front Panel.....	4.3
40-612 Programming Information	4.4
Relay Lookup Tables.....	4.8
Section 5	
Connector Pin Outs.....	5.1
Section 6	
Troubleshooting	6.1
Section 7	
Functional Description.....	7.1
Section 8	
Parts List	8.1
Section 9	
Caution	9.1

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SECTION 1 - INTRODUCTION

GENERAL

The 40-612 Very High Density Versatile Multiplexer module features a wide range of software selectable switching configurations. The 40-612 is especially useful where a high density MUX array is required that can adapt to different test configurations for different test targets, or where a test system may have to be reconfigured in the future. Typical applications include signal routing in ATE and data acquisition systems. The 40-612 module uses high quality electro-mechanical relays, connections are made via a front panel 160 pin DIN41612 connector.

MUX Configurations

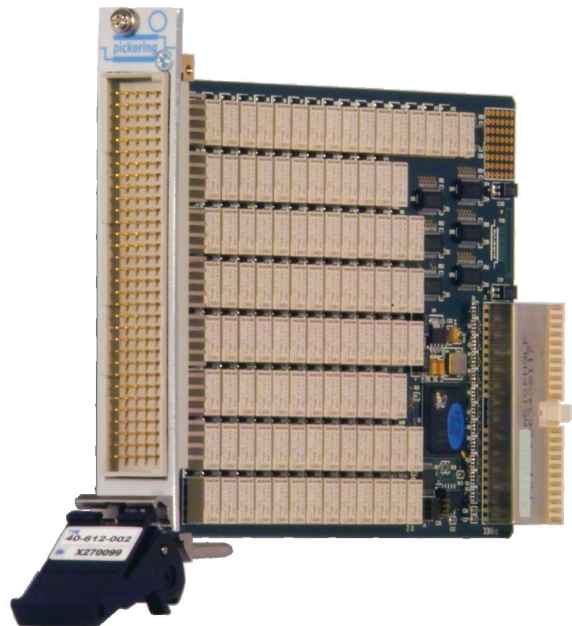
The module can be software configured into one of a large number of different multiplexer modes. Relays allow the multiplexer banks to be set in 1 or 2 pole mode and inter-bank switching enables the channel count to be increased up to a maximum of 128 (refer to Figure 1.1 overleaf).

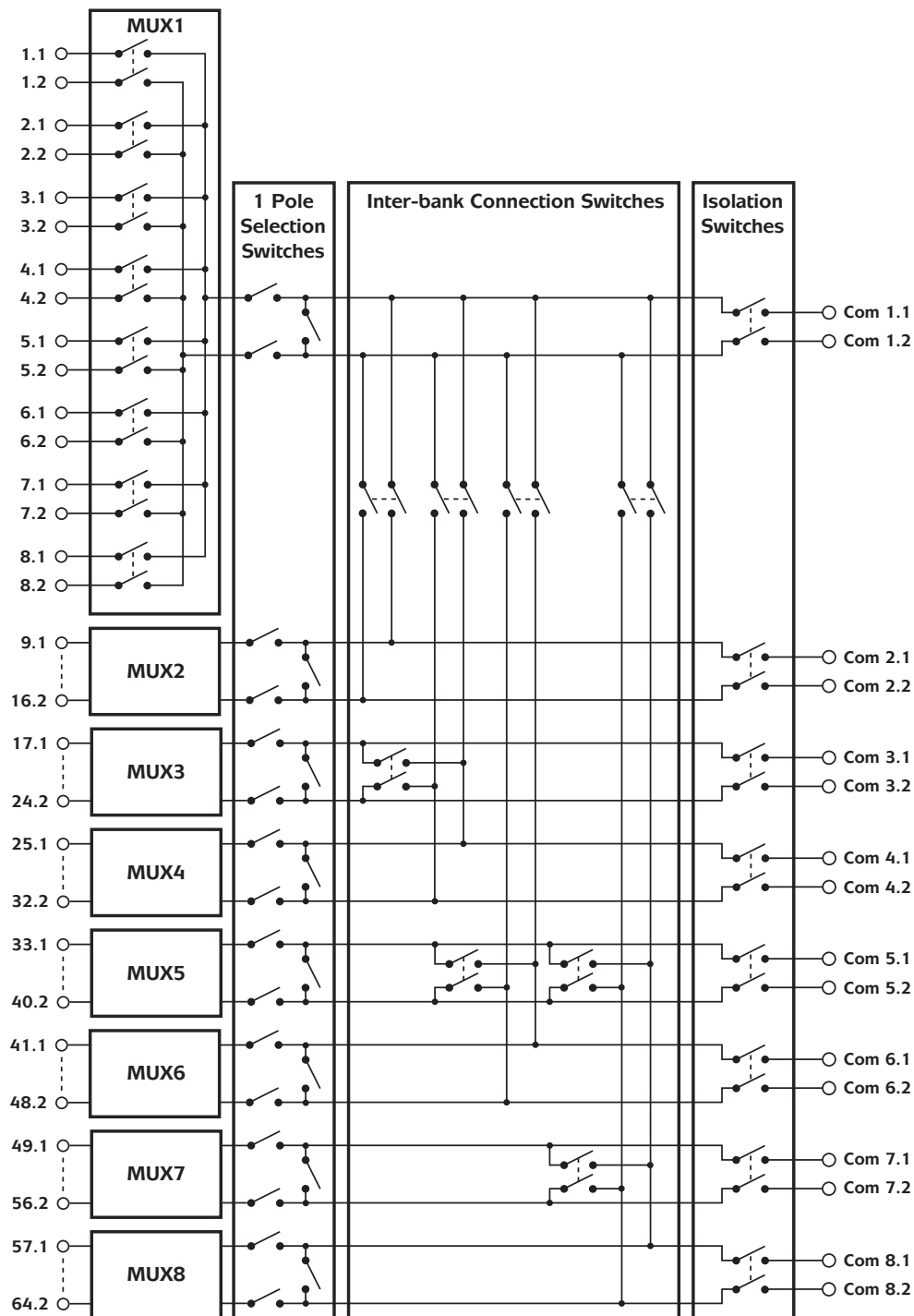
The versatility of the 40-612's architecture allows all multiplexer banks to be inter-linked and common connections used as extra signal inputs, creating a 71-channel 2-pole multiplexer. The 40-612 multiplexer may be operated as a conventional multiplexer with break-before-make action when a new channel is selected. For 2-pole configurations multiple channels can be simultaneously selected without restriction, for 1-pole configurations the channels that can be simultaneously selected are limited by the use of 2-pole relays.

Isolation Switching connects only the currently active multiplexer bank to the analog common, thereby keeping capacitive loading and leakage currents in large multiplexer systems to a minimum. Larger multiplexers may be constructed by Daisy Chaining the common signals from multiple PXI modules.

Some example multiplexer formats are as follows:

- 8 Banks 16 Channel 1 Pole
- 8 Banks 8 Channel 2 Pole
- 4 Banks 32 Channel 1 Pole
- 4 Banks 16 Channel 2 Pole
- 2 Banks 64 Channel 1 Pole
- 2 Banks 32 Channel 2 Pole
- 1 Banks 128 Channel 1 Pole
- 1 Banks 64 Channel 2 Pole





**Figure 1.1 - Very High Density Versatile Multiplexer Module 40-612:
Configuration Schematic**

SECTION 2 - SPECIFICATION

Relay Type

The 40-612 is fitted with electro-mechanical double pole relays, Palladium-Ruthenium Gold covered contacts. A **Spare Relay** is built onto the circuit board to facilitate easy maintenance with minimum downtime.

Programming

Pickering provide kernel, VISA and IVI drivers which are compatible with Windows 2000/XP operating systems, the VISA driver is also compatible with the LabVIEW RT operating system.

These drivers may be used with a variety of programming environments and applications including:

National Instruments products (LabVIEW/LabWindows/CVI/Switch Executive/MAX/TestStand etc.)

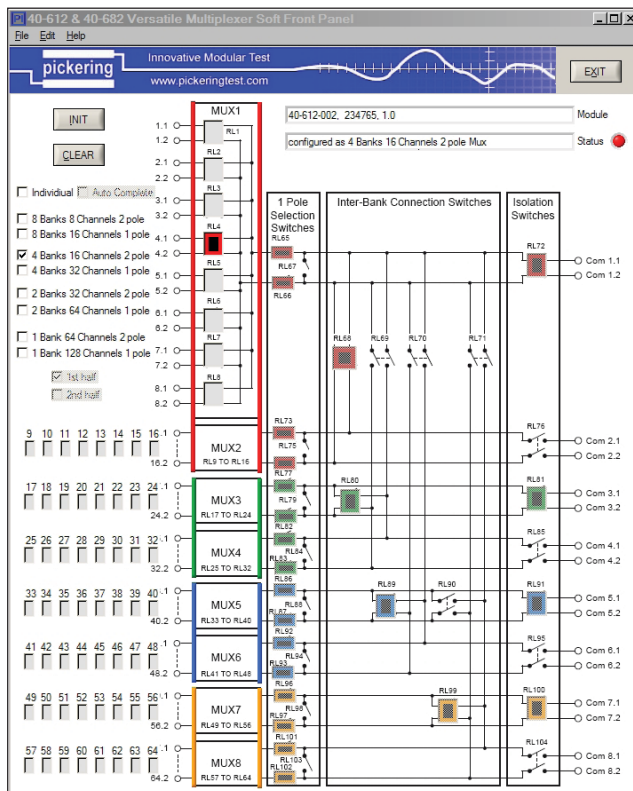
Microsoft Visual Studio products (Visual Basic/Visual C+)

Agilent VEE

Mathworks Matlab

Other environments are also supported, please contact Pickering with specific enquiries.

The Versatile Multiplexer Soft Front Panel for the 40-612-002 and 40-682-002 allows easy setting of various configurations from 8-bank 8-channels 2-pole multiplexers, up to 1-bank 128-channels 1-pole multiplexers as well as individual relay control for custom configurations. The schematic in the background of the SFP simplifies understanding of the selected topology. During configuration setting, all relay control information is logged in a text file which can be re-used in a programming environment.



Soft Front Panel for the 40-612 and 40-682 Very High Density Versatile Multiplexers

Switching Specification

Switch Type	Electro-mechanical
Contact Type:	Palladium-Ruthenium, Gold Covered Bifurcated
Max Switch Voltage:	300Vdc/250Vac
Max Power:	60W/62.5VA
Max Switch Current:	2A
Max Carry Current:	2A
Path Resistance - On:	500mΩ max, 300mΩ typ †
Path Resistance - Off:	>10 ⁹ Ω
Minimum Voltage:	100μV
Thermal Offset:	<10μV †
Operate Time:	<3ms
Expected Life (operations)	
Very low power signal load:	>1x10 ⁸
Low power load (2W):	>1.5x10 ⁷ (0.1A 20Vdc)
Medium power load (30W):	>5x10 ⁶ (1A 30Vdc)
Full power load (60W):	>1x10 ⁵ (2A 30Vdc)
	>1x10 ⁵ (0.2A 300Vdc)

† Path resistance & thermal offset are dependent upon the signal route selected.

Power Requirements

+3.3V	+5V	+12V	-12V
5mA	2A max (typ 280mA)	0	0

Width and Dimensions

Single slot 3U PXI (CompactPCI card).

PXI & CompactPCI Compliance

All Pickering Interfaces PXI modules comply with the PXI Specification 2.2. Local Bus, Interrupts, Trigger Bus and Star Trigger are not implemented.

Compatible with PXI Express Hybrid Slot

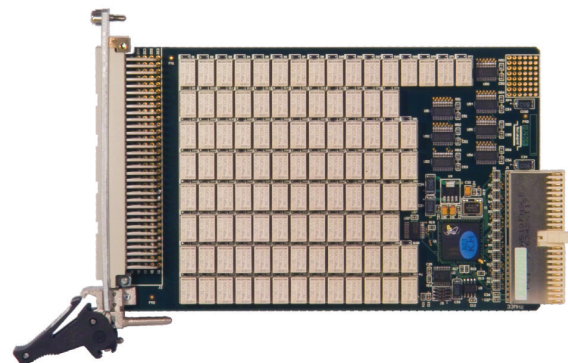
Safety & CE Compliance

All modules are fully CE compliant and meet applicable EU directives: Low-voltage safety EN61010-1:2001, EMC Immunity EN61000-6-1:2001, Emissions EN55011:1998.

Connectors

Signals via front panel 160 way DIN41612 male connector, for pin outs please refer to the operating manual.

We recommend that Pickering mating connectors are used with this module which are designed to ensure there are no mechanical interference problems when used in a PXI chassis.



PCB Layout for the 40-612-002 Very High Density Versatile MUX

Product Order Codes

8 Bank, 8 Channel, 2 Pole
Versatile Multiplexer Module **40-612-002**

Mating Connectors & Cabling

To ensure the best performance from the 40-612, connectors and cabling from Pickering are recommended as these include specially designed strain relief fixings:

40-960-160 160 way, 2A, crimp pin connector.

40-970-160-1M Cableform, 160 way DIN41612 Style, Female to Female, 2A, 1m Length.

40-967-160 DIN Rail Breakout, 160 way DIN41612 Style plug, to screw terminals.

Please refer to the Pickering Interfaces “Interconnection Solutions” catalog for the full list of connector/cabling options, including drawings, photos and specifications. This is available in either print or as a download. Alternatively our web site has dynamically linked connector/cabling options, including pricing, for all Pickering PXI modules.



Latest Details

Please refer to our Web Site for Latest Product Details.

www.pickeringtest.com

Operating/Storage Conditions

Operating Conditions

Operating Temperature: 0°C to 55°C
Humidity: Up to 90% non-condensing
Altitude: 5000m

Storage and Transport Conditions

Storage Temperature: -20°C to +75°C
Humidity: Up to 90% non-condensing
Altitude: 15000m

SECTION 3 - INSTALLATION

SOFTWARE INSTALLATION

First install the appropriate Pickering PXI switch card drivers by running the installer program Setup.exe, either from the CD-ROM supplied, or by downloading the latest version from our website <http://www.pickeringtest.com> - the recommended method. There are different versions of the Setup program to suit different Windows versions and software environments. Setup is accompanied by a ReadMe file containing additional installation information. A single installation covers all cards in the System 40, System 45 and System 50 ranges.

When installation completes, the installed drivers' ReadMe file is offered for display. It can also be displayed later using a shortcut on the Programs>>Pickering menu.

If you are not a LabVIEW user you should choose the "full" version, and once that has been installed run the LabVIEW Runtime Engine installer via the shortcut on the Programs>>Pickering menu. In the absence of LabVIEW the Runtime Engine is required to support the Pickering Test Panels application.

HARDWARE INSTALLATION

CAUTION

Electrostatic discharge can damage the components on the module. To avoid such damage in handling the board, touch the anti-static bag to a metal part of the chassis before removing the board from the bag.

Ensure that there is adequate ventilation in accordance with the PXI Specification.

The module should be installed in accordance with the following procedure:

1. Ensure that the system is turned OFF but still connected to mains so that it remains grounded.
2. Choose an appropriate slot in the rack.
3. Remove the blanking plate for the chosen slot.
4. Ensure that the injector/ejector handle is in its downward position. Align the module with the card guides on the top and bottom of the slot.

CAUTION

Do not raise the injector/ejector handle whilst inserting the module. The module will not insert properly unless the handle is in its downward position.

5. Hold the handle whilst slowly sliding the module into the card guides until the handle catches on the injector/ejector rail (refer to Figure 3.1).
6. Raise the injector/ejector handle until the module firmly seats into the backplane. The front panel of the module should be flush with the front panel of the chassis.
7. Screw the front panel of the module to the front panel mounting rail.
8. In a system employing MXI-3 to connect a desktop PC to a PXI chassis or to link multiple chassis, power-up the system as follows:
 - a. For a system comprising a PC and one chassis, power up the chassis before powering up the PC.
 - b. For a system comprising more than one chassis, turn ON the last chassis in the system followed by the penultimate, etc, and finally turn ON the PC or chassis containing the system controller.

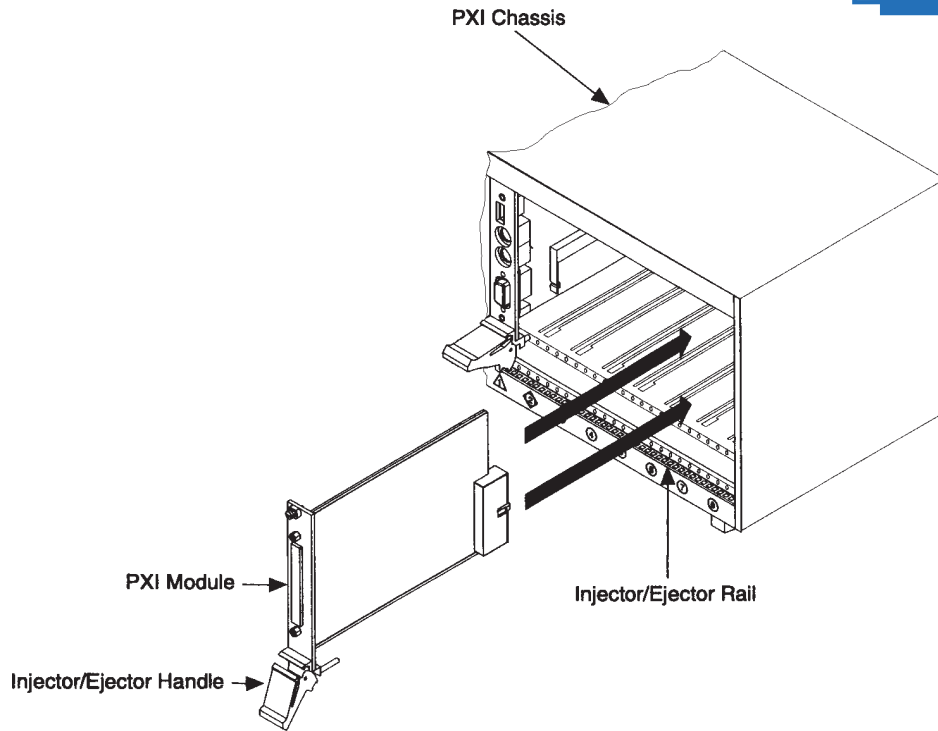


Figure 3.1 - Installing the module into a PXI/Compact PCI Chassis

TESTING OPERATION

Start the Test Panels application from the Programs>>Pickering>>PXI Utilities menu. If you are a LabVIEW user, run "Test Panels (LabVIEW VI)"; if not, run "Test Panels (EXE)". A selector panel will appear, listing all installed Pickering PXI switch cards. Click on the card you wish to control, and a graphical control panel is presented allowing operation of the card. Panels can be opened simultaneously for all the installed cards.

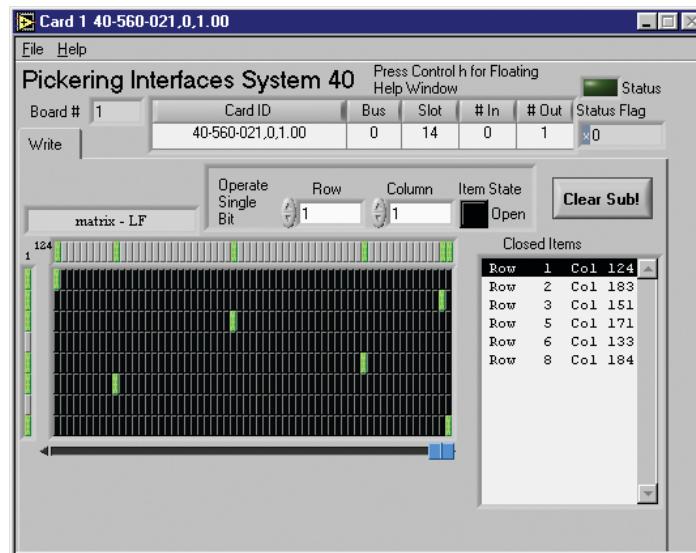


Figure 3.2 - Typical Test Panel Display

As an alternative to the Test Panels, the simple Terminal Monitor program PILMon (again on the Programs>>Pickering>>PXI Utilities menu) allows access to all functions of Pickering switch cards through a command-line interface. In PILMon, enter "HE" for help on it's commands.

Please note that both the Test Panels and Terminal Monitor gain exclusive access to the cards, and so only one of them can be operational at any time.

SECTION 4 - PROGRAMMING

Programming options for Pickering Interfaces PXI Cards

Software drivers are supplied for Microsoft Windows 2000/XP operating systems, with specific support for the following development environments:

- Microsoft Visual Basic
- Microsoft Visual C++
- Borland C++
- National Instruments LabWindows/CVI
- National Instruments LabVIEW and LabVIEW RT

Windows drivers are supplied in the form of Dynamic Link Libraries, which should also be usable in any other development environment that supports them.

Three different Windows drivers are available to meet particular system requirements, and should none of these be suitable there is also the option of register-level programming. Drivers are generally 'universal', handling all models in the System 40, 45 and 50 ranges; however some models that are not compliant with the Iviswch class cannot be used with the pi40iv IVI driver. The pipx40 and Pilpxi drivers are also applicable to certain models in the System 41 (PXI Instruments) range - see these drivers' System 41 support lists.

Please note that this documentation is available in its most up-to-date form as HTML help files, fully hyperlinked for easy access - both pipx40 and Pilpxi documents are included in the Pipx40vpp software installation.

IVI Driver for Windows - pi40iv

The pi40iv IVI (Interchangeable Virtual Instrument) driver supports all Pickering Interfaces PXI switch cards that are consistent with the Iviswch class model - as are the great majority of cards in the System 40/45/50 ranges. It integrates well with LabWindows/CVI and LabVIEW, and is fully compatible with Switch Executive. It is also usable in general-purpose programming environments such as Visual C++ and Visual Basic.

Prior installation of the VISA and IviEngine from National Instruments is required for the correct installation and operation of this driver.

VISA Driver for Windows - pipx40

The pipx40 driver conforms to the VISA (Virtual Instrument Software Architecture) standard for programmable instrumentation. Instrument control environments such as LabVIEW and LabWindows/CVI are based on VISA, and pipx40 support libraries are provided for them.

Prior installation of VISA from National Instruments is required for the operation of this driver.

Where VISA is available, pipx40 can also be used in general-purpose programming environments such as Visual C++ and Visual Basic. When IVI is not a system requirement this driver will often yield faster operation than the pi40iv driver.

Direct I/O Driver for Windows - Pilpxi

The Pilpxi driver accesses cards directly, without using the VISA software layer, while offering similar overall functionality to pipx40. It is most commonly used in general-purpose programming environments such as Visual C++ and Visual Basic. Operating speed of the VISA and Direct I/O drivers is generally comparable.

Register-level Programming

Where the supplied drivers are not suitable, register-level programming can be employed - for example:

- If the functionality of the supplied drivers does not meet the application requirements.
- If security considerations demand full source-code for the application.
- In development environments that have alternate mechanisms for accessing PCibus.
- For operating systems other than Windows LabVIEW, LabWindows/CVI and Switch Executive are trademarks of National Instruments Corporation.

Details of the above drivers is available in separate documentation.

Card Architecture

Sub-units

Pickering PXI cards contain one or more independently addressable functional blocks, or sub-units. Sub-unit numbers begin at 1, and separate sequences are used for input and output functions. This number is used in function calls to access the appropriate block. Generally, sub-unit numbers correspond directly to the bank numbers specified in hardware documentation.

Sub-unit examples:

Model	Configuration	INPUT sub-unit #1	OUTPUT sub-unit #1	OUTPUT sub-unit #2	OUTPUT sub-unit #3
40-110-021	16 SPDT switches	None	16 SPDT switches	None	None
40-290-121	Dual Programmable resistors + 16 SPDT switches	None	Resistor #1	Resistor #2	16 SPDT switches
40-490-001	Digital I/O	16-channel inputs	32-channel outputs	None	None
40-511-021	Dual 12 x 4 matrix	None	12 x 4 matrix #1	12 x 4 matrix #2	None

Sub-unit characteristics

The numbers of input and output sub-units in a card can be obtained using functions from the libraries:

pipx40 pipx40_getSubCounts

pilpxi PIL_EnumerateSubs

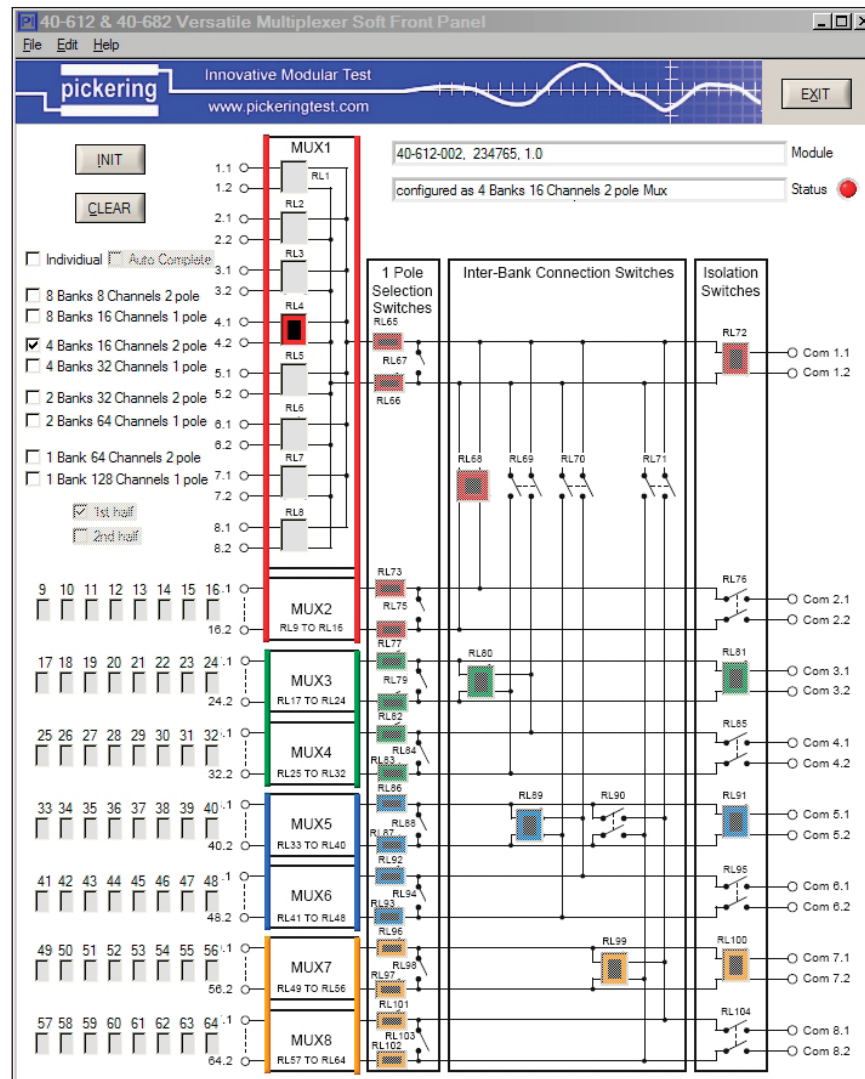
pipx40 pipx40_getSubType, pipx40_getSubInfo

pilpxi PIL_SubType, PIL_SubInfo

For further detail of how to access and use Pickering drivers the user is advised to refer to the documentation provided with the installed drivers.

Soft Front Panel

The Versatile Multiplexer Soft Front Panel for the 40-612-002 and 40-682-002 allows easy setting of various configurations from 8-bank 8-channels 2-pole multiplexers, up to 1-bank 128-channels 1-pole multiplexers as well as individual relay control for custom configurations. The schematic in the background of the SFP simplifies understanding of the selected topology. During configuration setting, all relay control information is logged in a text file which can be re-used in a programming environment.



Soft Front Panel for the 40-612 and 40-682 Very High Density Versatile Multiplexers

40-612 Programming Information

Sub-unit Information

This card is a versatile MUX card and may be programmatically modified to many different configurations.

In it's basic state it performs as a 8 banks of 2-wire 8x1 MUX units, with additional switching these banks may be connected together to form MUXes of larger size, for example 16x1, 24, 1, 32x1 etc. It is also possible to use the 2-wires as individual inputs, changing a 2-wire 8x1 section into a 1-wire 16x1.

In terms of sub-units, discussed briefly in the preceding section, the 40-612 contains 13 sub-units as follows:

Sub-Unit	Size	Use
1 thro 8	8 bits	2-wire 8x1 MUX on each sub-unit
9	8 bits	output isolator switches
10	8 bits	pole 1 selection
11	8 bits	pole 2 selection
12	8 bits	pole shorting
13	8 bits	inter-bank linking switches

Table 4.9 describes the function of each bit in each sub-unit.

Figure 4.1 shows a schematic of the switch wiring on the card.

Card Configurations

2 wire, 8 off 8x1 MUX Use

In order to use the card as the basic 2-wire, 8 off, 8x1 MUX the switches should be set as follows:

Sub-unit 10 and 11 should both be set to hex ff to energise all the pole selection relays.

Sub-unit 12 should be set to hex 00 to leave the shorting relays un-energised

Sub-unit 13 should be set to hex 00 to leave all inter-bank linking relays un-energised

Then inputs are selected on sub-units 1 thro 8 and the appropriate output isolation selected on sub-unit 9 to route the paths to the output pins.

Building Wider MUX Units

To transform the card into a 2-wire, 4 off, 16x1 MUX, proceed as follows:

Energise RL68 to connect bank 1 to bank 2

Energise RL80 to connect bank 3 to bank 4

Energise RL89 to connect bank 5 to bank 6

Energise RL99 to connect bank 7 to bank 8

To do this, energise bits 1, 5, 6 and 7 in sub-unit 13.

Now sub-units 1 and 2 control the 16 inputs to the first 16x1 MUX, sub-units 3 and 4 the second 16x1 MUX etc.

Sub-unit 10 and 11 should both be set to hex ff to energise all the pole selection relays.

Sub-unit 12 should be set to hex 00 to leave the shorting relays un-energised

Sub-unit 9 is used to connect the MUX to the output pins, now however, due to the linking, there is a choice of 2 possible output locations, or indeed both simultaneously. Setting bit 1 will connect the 16x1 MUX to output Com1.1/2, selecting bit 2 will connect to Com2.1/2.

Use as a 1-wire MUX

Appropriate switch configuration can allow a 2-wire 8x1 MUX to operate as a 1-wire 16x1 MUX.

The 16 inputs are connected to the 8x2 wires of the MUX. Then the pole selection relays are used to select which input path is routed to the output section. The user may choose to either wire together Com1.1 and Com1.2, or energise the pole shorting relay to route both poles to both outputs, or use one output channel and alternate energisation of the shorting relay to route the required input to the output.

Both these techniques may be used in any combination resulting in a very large number of possible configurations varying from the basic 2-wire, 8 off, 8x1 MUX, to a 2-wire 1 off 64x1 MUX, to a 1-wire, 1 off 128x1 MUX, or any possible combination.

Examples using the 3 main PXI drivers available are shown on the following pages.

Direct IO Driver pilpxi - Setting card to 2-wire, 4 off, 16x1 MUX

```
DWORD card;
DWORD data[1];

PIL_OpenSpecifiedCard(4, 15, &card);

// Configure for 2-wire, 4-off, 16x1 MUX

// First set the linking switches to link adjacent banks

// using OpBit commands to set individual bits
PIL_ClearSub(card, 13);
PIL_OpBit(card, 13, 1, 1);
PIL_OpBit(card, 13, 5, 1);
PIL_OpBit(card, 13, 6, 1);
PIL_OpBit(card, 13, 7, 1);

/* or using WriteSub command to set entire sub-unit

data = 0x71;
PIL_WriteSub(card, 13, data);

*/

// Now energise all the pole selection relays

data[0] = 0xFF;
PIL_WriteSub(card, 10, data);
PIL_WriteSub(card, 11, data);

// Then make sure the pole shorting relays are un-energised

data[0] = 0x00;
PIL_WriteSub(card, 12, data);

// Connect all the output isolation relays

data[0] = 0xFF;

PIL_WriteSub(card, 9, data);

// Select input 1 of first 16x1 MUX (1st bit on first 8x1 bank)

PIL_OpBit(card, 1, 1, 1);

// Select input 9 of first 16x1 MUX (1st bit on 2nd 8x1 bank)

PIL_OpBit(card, 2, 1, 1);

PIL_CloseSpecifiedCard(card);
```

VISA Driver pipx40 - Setting card to 2-wire, 4 off, 16x1 MUX

```
ViSession vi;
ViUInt32 data[1];

pipx40_init("PXI4::15::INSTR", 0, 0, &vi);

// Configure for 2-wire, 4-off, 16x1 MUX

// First set the linking switches to link adjacent banks

// using setChannelState commands to set individual bits
pipx40_clearSub(card, 13);
pipx40_setChannelState(vi, 13, 1, 1);
pipx40_setChannelState(vi, 13, 5, 1);
pipx40_setChannelState(vi, 13, 6, 1);
pipx40_setChannelState(vi, 13, 7, 1);

/* or using setChannelPattern command to set entire sub-unit

data = 0x71;

pipx40_setChannelPattern(vi,13, data);

*/

// Now energise all the pole selection relays

data[0] = 0xFF;
pipx40_setChannelPattern(vi,10, data);
pipx40_setChannelPattern(vi,11, data);

// Then make sure the pole shorting relays are un-energised

data[0] = 0x00;
pipx40_setChannelPattern(vi,12, data);

// Connect all the output isolation relays

data[0] = 0xFF;
pipx40_setChannelPattern(vi,9, data);

// Select input 1 of first 16x1 MUX (1st bit on first 8x1 bank)

pipx40_setChannelState(vi, 1, 1, 1);

// Select input 9 of first 16x1 MUX (1st bit on 2nd 8x1 bank)

pipx40_setChannelState(vi, 2, 1, 1);

pipx40_close(vi);
```

IVI Driver

The IVI-C driver pi40iv has been coded to cope with the versatility of this card and has a number of common configurations included in its card definition file. This relieves the user of the complexity of deciding which switches need be in what state and totally automates the process.

The following configurations are provided in the pi40iv.ini driver configuration file in your installation. Use one of these strings in the InitWithOptions function.

```
40-612-002
40-612-002-2w8/8x1
40-612-002-2w4/16x1
40-612-002-2w2/32x1
40-612-002-1w16/8x1
40-612-002-1w8/16x1
40-612-002-1w4/32x1
40-612-002-1w2/64x1
40-612-002-1w128x1
```

The driver will initialise the card in the desired configuration, allocate suitable channel names for that configuration and deal with all the switching complexities detailed above.

For example:

```
ViRsrc rsrc = "PXI4::15::INSTR";

ViString opt = "Simulate=1," \
               "RangeCheck=1," \
               "QueryInstrStatus=1," \
               "Cache=1," \
               "DriverSetup=Model:40-612-002-2w4/16x1;";

pi40iv_InitWithOptions(rsrc, VI_TRUE, VI_TRUE, opt, &vi);
```

Will lead to channel names	"comA" and "chA1" thro "chA16"
	"comB" and "chB1" thro "chB16"
	"comC" and "chC1" thro "chC16"
	"comD" and "chD1" thro "chD16"

Other configurations are possible, refer to the pi40iv programming manual in your installation folder, or contact support@pickeringinttest.com for details.

Relay Look-up Tables

Tables 4.1 to 4.8 provide relay look-up tables. Tables 4.9 to 4.11 provide programming information.

TABLE 4.1 - 8 Banks 16 Channel 1-pole Relay Look-Up Table

Bank	Relays Operated			
	1/2-pole	Interbank	Isolation	Channel Selection
1	67 (c) & 66 (.2) or only 65 (.1)*	Not Applicable	72	1, 2, 3, 4, 5, 6, 7, 8
2	75 (c) & 74 (.2) or only 73 (.1)*	Not Applicable	76	9, 10, 11, 12, 13, 14, 15, 16
3	79 (c) & 78 (.2) or only 77 (.1)*	Not Applicable	81	17, 18, 19, 20, 21, 22, 23, 24
4	84 (c) & 83 (.2) or only 82 (.1)*	Not Applicable	85	25, 26, 27, 28, 29, 30, 31, 32
5	88 (c) & 87 (.2) or only 86 (.1)*	Not Applicable	91	33, 34, 35, 36, 37, 38, 39, 40
6	94 (c) & 93 (.2) or only 92 (.1)*	Not Applicable	95	41, 42, 43, 44, 45, 46, 47, 48
7	98 (c) & 97 (.2) or only 96 (.1)*	Not Applicable	100	49, 50, 51, 52, 53, 54, 55, 56
8	103 (c) & 102 (.2) or only 101 (.1)*	Not Applicable	104	57, 58, 59, 60, 61, 62, 63, 64

TABLE 4.2 - 8 Banks 8 Channel 2-pole Relay Look-Up Table

Bank	Relays Operated			
	1/2-pole	Interbank	Isolation	Channel Selection
1	65, 66	Not Applicable	72	1, 2, 3, 4, 5, 6, 7, 8
2	73, 74	Not Applicable	76	9, 10, 11, 12, 13, 14, 15, 16
3	77, 78	Not Applicable	81	17, 18, 19, 20, 21, 22, 23, 24
4	82, 83	Not Applicable	85	25, 26, 27, 28, 29, 30, 31, 32
5	86, 87	Not Applicable	91	33, 34, 35, 36, 37, 38, 39, 40
6	92, 93	Not Applicable	95	41, 42, 43, 44, 45, 46, 47, 48
7	96, 97	Not Applicable	100	49, 50, 51, 52, 53, 54, 55, 56
8	101, 102	Not Applicable	104	57, 58, 59, 60, 61, 62, 63, 64

TABLE 4.3 - 4 Banks 32 Channel 1-pole Relay Look-Up Table

Bank	Relays Operated			
	1/2-pole	Interbank	Isolation	Channel Selection
1	"67 (c) & 66 (.2) or only 65 (.1)* and 75 (c) & 74 (.2) or only 73 (.1)*"	68	72	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16
2	"79 (c) & 78 (.2) or only 77 (.1) * and 84 (c) & 83 (.2) or only 82 (.1)*"	80	81	17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32
3	"88 (c) & 87 (.2) or only 86 (.1)* and 94 (c) & 93 (.2) or only 92 (.1)*"	89	91	33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48
4	"98 (c) & 97 (.2) or only 96 (.1) * and 103 (c) & 102 (.2) or only 101 (.1)*"	99	100	49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64

TABLE 4.4 - 4 Banks 16 Channel 2-pole Relay Look-Up Table

Bank	Relays Operated			
	1/2-pole	Interbank	Isolation	Channel Selection
1	65, 66, 73, 74	68	72	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16
2	77, 78, 82, 83	80	81	17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32
3	86, 87, 92, 93	89	91	33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48
4	96, 97, 101, 102	99	100	49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64

TABLE 4.5 - 2 Banks 64 Channel 1-pole Relay Look-Up Table

Bank	Relays Operated			
	1/2-pole	Interbank	Isolation	Channel Selection
1	"67 (c) & 66 (.2) or only 65 (.1)* and 75 (c) & 74 (.2) or only 73 (.1)* and 79 (c) & 78 (.2) or only 77 (.1) * and 84 (c) & 83 (.2) or only 82 (.1)*"	68, 69, 80	72	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32
2	"88 (c) & 87 (.2) or only 86 (.1)* and 94 (c) & 93 (.2) or only 92 (.1)* and 98 (c) & 97 (.2) or only 96 (.1) * and 103 (c) & 102 (.2) or only 101 (.1)*"	89, 90, 99	91	33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64

TABLE 4.6 - 2 Banks 32 Channel 2-pole Relay Look-Up Table

Bank	Relays Operated			
	1/2-pole	Interbank	Isolation	Channel Selection
1	65, 66, 73, 74, 77, 78, 82, 83	68, 69, 80	72	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32
2	86, 87, 92, 93, 96, 97, 101, 102	89, 90, 99	91	33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64

TABLE 4.7 - 1 Bank 128 Channel 1-pole Relay Look-Up Table

Bank	Relays Operated			
	1/2-pole	Interbank	Isolation	Channel Selection
1	"67 (c) & 66 (.2) or only 65 (.1)* and 75 (c) & 74 (.2) or only 73 (.1)* and 79 (c) & 78 (.2) or only 77 (.1) * and 84 (c) & 83 (.2) or only 82 (.1)* and 88 (c) & 87 (.2) or only 86 (.1)* and 94 (c) & 93 (.2) or only 92 (.1)* and 98 (c) & 97 (.2) or only 96 (.1) * and 103 (c) & 102 (.2) or only 101 (.1)*"	68, 69, 70, 71, 80, 89, 90, 99	72	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64

TABLE 4.8 - 1 Bank 64 Channel 2-pole Relay Look-Up Table

Bank	Relays Operated			
	1/2-pole	Interbank	Isolation	Channel Selection
1	"65, 66, 73, 74, 77, 78, 82, 83, 86, 87, 92, 93, 96, 97, 101, 102"	68, 69, 70, 71, 80, 89, 90, 99	72	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64

* = To prevent signals on the .1 & .2 mux's being shorted together either the .1 or .2 relay should be operated in 1-pole mode depending on where the signal originates. The common (c) relay is used to route the .2 mux signals to the .1 common output pin on the module connector and can remain de-energised when signals from the .1 sections are used in 1-pole mode.

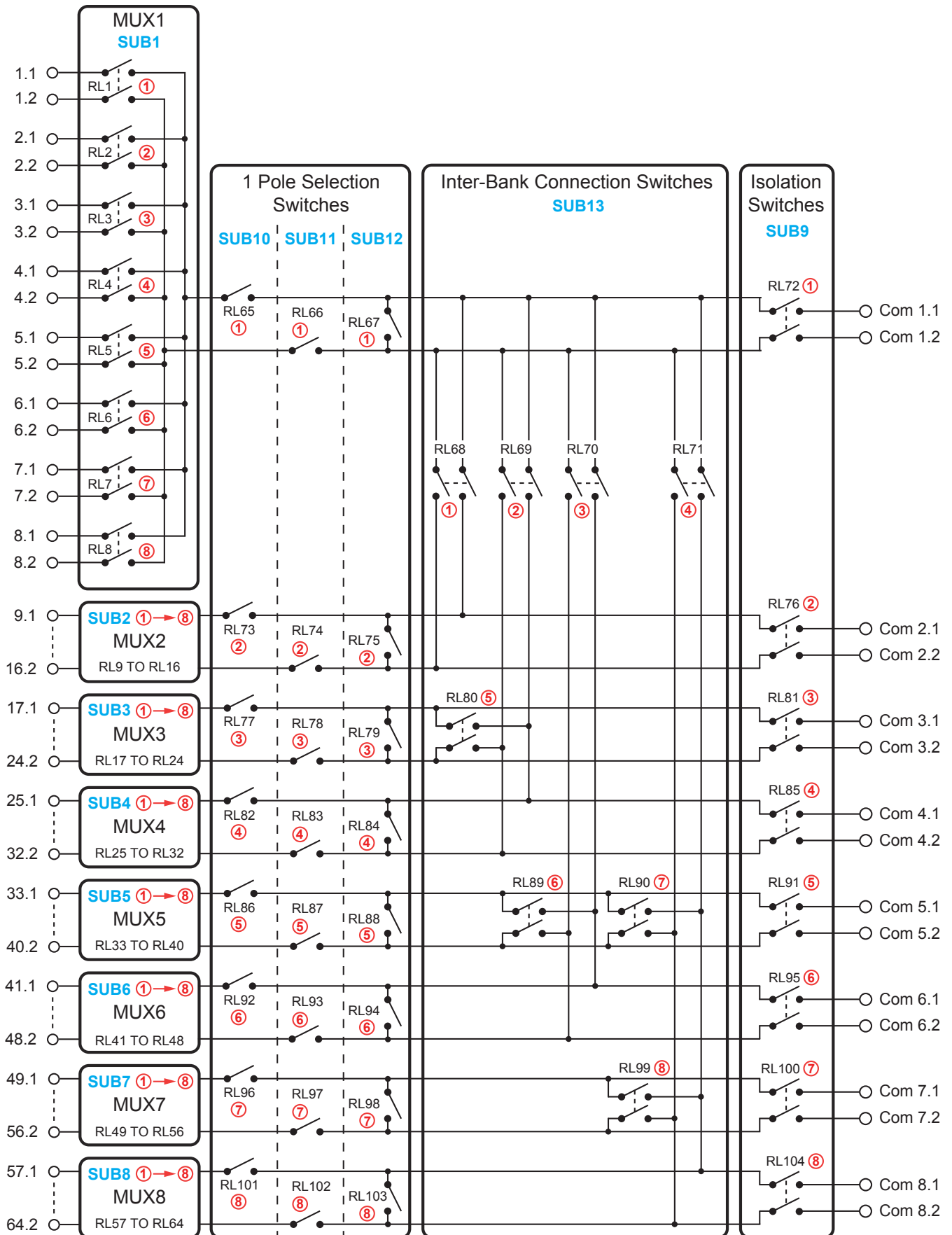


Figure 4.1 - Relay Switching Schematic, programming sub-unit numbers are in blue, bit numbers within a sub-unit are in circled in red.

TABLE 4.9 Physical Relay To Software Sub-Unit Cross Reference

Logical Sub-Unit	Sub-unit Type	Logical Chan	Switch Function	Bank	Channel	Function	Relay (RL)
1	MUXM(8)	1	Channel	1	1	Bank 1, Channel 1	1
1	MUXM(8)	2	Channel	1	2	Bank 1, Channel 2	2
1	MUXM(8)	3	Channel	1	3	Bank 1, Channel 3	3
1	MUXM(8)	4	Channel	1	4	Bank 1, Channel 4	4
1	MUXM(8)	5	Channel	1	5	Bank 1, Channel 5	5
1	MUXM(8)	6	Channel	1	6	Bank 1, Channel 6	6
1	MUXM(8)	7	Channel	1	7	Bank 1, Channel 7	7
1	MUXM(8)	8	Channel	1	8	Bank 1, Channel 8	8
2	MUXM(8)	1	Channel	2	1	Bank 2, Channel 1	9
2	MUXM(8)	2	Channel	2	2	Bank 2, Channel 2	10
2	MUXM(8)	3	Channel	2	3	Bank 2, Channel 3	11
2	MUXM(8)	4	Channel	2	4	Bank 2, Channel 4	12
2	MUXM(8)	5	Channel	2	5	Bank 2, Channel 5	13
2	MUXM(8)	6	Channel	2	6	Bank 2, Channel 6	14
2	MUXM(8)	7	Channel	2	7	Bank 2, Channel 7	15
2	MUXM(8)	8	Channel	2	8	Bank 2, Channel 8	16
3	MUXM(8)	1	Channel	3	1	Bank 3, Channel 1	17
3	MUXM(8)	2	Channel	3	2	Bank 3, Channel 2	18
3	MUXM(8)	3	Channel	3	3	Bank 3, Channel 3	19
3	MUXM(8)	4	Channel	3	4	Bank 3, Channel 4	20
3	MUXM(8)	5	Channel	3	5	Bank 3, Channel 5	21
3	MUXM(8)	6	Channel	3	6	Bank 3, Channel 6	22
3	MUXM(8)	7	Channel	3	7	Bank 3, Channel 7	23
3	MUXM(8)	8	Channel	3	8	Bank 3, Channel 8	24
4	MUXM(8)	1	Channel	4	1	Bank 4, Channel 1	25
4	MUXM(8)	2	Channel	4	2	Bank 4, Channel 2	26
4	MUXM(8)	3	Channel	4	3	Bank 4, Channel 3	27
4	MUXM(8)	4	Channel	4	4	Bank 4, Channel 4	28
4	MUXM(8)	5	Channel	4	5	Bank 4, Channel 5	29
4	MUXM(8)	6	Channel	4	6	Bank 4, Channel 6	30
4	MUXM(8)	7	Channel	4	7	Bank 4, Channel 7	31
4	MUXM(8)	8	Channel	4	8	Bank 4, Channel 8	32

TABLE 4.9 Physical Relay To Software Sub-Unit Cross Reference (continued)

Logical Sub-Unit	Sub-unit Type	Logical Chan	Switch Function	Bank	Channel	Function	Relay (RL)
5	MUXM(8)	1	Channel	5	1	Bank 5, Channel 1	33
5	MUXM(8)	2	Channel	5	2	Bank 5, Channel 2	34
5	MUXM(8)	3	Channel	5	3	Bank 5, Channel 3	35
5	MUXM(8)	4	Channel	5	4	Bank 5, Channel 4	36
5	MUXM(8)	5	Channel	5	5	Bank 5, Channel 5	37
5	MUXM(8)	6	Channel	5	6	Bank 5, Channel 6	38
5	MUXM(8)	7	Channel	5	7	Bank 5, Channel 7	39
5	MUXM(8)	8	Channel	5	8	Bank 5, Channel 8	40
6	MUXM(8)	1	Channel	6	1	Bank 6, Channel 1	41
6	MUXM(8)	2	Channel	6	2	Bank 6, Channel 2	42
6	MUXM(8)	3	Channel	6	3	Bank 6, Channel 3	43
6	MUXM(8)	4	Channel	6	4	Bank 6, Channel 4	44
6	MUXM(8)	5	Channel	6	5	Bank 6, Channel 5	45
6	MUXM(8)	6	Channel	6	6	Bank 6, Channel 6	46
6	MUXM(8)	7	Channel	6	7	Bank 6, Channel 7	47
6	MUXM(8)	8	Channel	6	8	Bank 6, Channel 8	48
7	MUXM(8)	1	Channel	7	1	Bank 7, Channel 1	49
7	MUXM(8)	2	Channel	7	2	Bank 7, Channel 2	50
7	MUXM(8)	3	Channel	7	3	Bank 7, Channel 3	51
7	MUXM(8)	4	Channel	7	4	Bank 7, Channel 4	52
7	MUXM(8)	5	Channel	7	5	Bank 7, Channel 5	53
7	MUXM(8)	6	Channel	7	6	Bank 7, Channel 6	54
7	MUXM(8)	7	Channel	7	7	Bank 7, Channel 7	55
7	MUXM(8)	8	Channel	7	8	Bank 7, Channel 8	56
8	MUXM(8)	1	Channel	8	1	Bank 8, Channel 1	57
8	MUXM(8)	2	Channel	8	2	Bank 8, Channel 2	58
8	MUXM(8)	3	Channel	8	3	Bank 8, Channel 3	59
8	MUXM(8)	4	Channel	8	4	Bank 8, Channel 4	60
8	MUXM(8)	5	Channel	8	5	Bank 8, Channel 5	61
8	MUXM(8)	6	Channel	8	6	Bank 8, Channel 6	62
8	MUXM(8)	7	Channel	8	7	Bank 8, Channel 7	63
8	MUXM(8)	8	Channel	8	8	Bank 8, Channel 8	64

TABLE 4.9 Physical Relay To Software Sub-Unit Cross Reference (continued)

Logical Sub-Unit	Sub-unit Type	Logical Chan	Switch Function	Bank	Channel	Function	Relay (RL)
9	SWITCH(8)	1	Isolation	1	NA	Bank 1 isolation	72
9	SWITCH(8)	2	Isolation	2	NA	Bank 2 isolation	76
9	SWITCH(8)	3	Isolation	3	NA	Bank 3 isolation	81
9	SWITCH(8)	4	Isolation	4	NA	Bank 4 isolation	85
9	SWITCH(8)	5	Isolation	5	NA	Bank 5 isolation	91
9	SWITCH(8)	6	Isolation	6	NA	Bank 6 isolation	95
9	SWITCH(8)	7	Isolation	7	NA	Bank 7 isolation	100
9	SWITCH(8)	8	Isolation	8	NA	Bank 8 isolation	104
10	SWITCH(8)	1	1-Pole selection	1	NA	Bank 1 , 1/2-pole selection	65
10	SWITCH(8)	2	1-Pole selection	2	NA	Bank 2 , 1/2-pole selection	73
10	SWITCH(8)	3	1-Pole selection	3	NA	Bank 3 , 1/2-pole selection	77
10	SWITCH(8)	4	1-Pole selection	4	NA	Bank 4 , 1/2-pole selection	82
10	SWITCH(8)	5	1-Pole selection	5	NA	Bank 5 , 1/2-pole selection	86
10	SWITCH(8)	6	1-Pole selection	6	NA	Bank 6 , 1/2-pole selection	92
10	SWITCH(8)	7	1-Pole selection	7	NA	Bank 7 , 1/2-pole selection	96
10	SWITCH(8)	8	1-Pole selection	8	NA	Bank 8 , 1/2-pole selection	101
11	SWITCH(8)	1	2-Pole selection	1	NA	Bank 1 , 1/2-pole selection	66
11	SWITCH(8)	2	2-Pole selection	2	NA	Bank 2 , 1/2-pole selection	74
11	SWITCH(8)	3	2-Pole selection	3	NA	Bank 3 , 1/2-pole selection	78
11	SWITCH(8)	4	2-Pole selection	4	NA	Bank 4 , 1/2-pole selection	83
11	SWITCH(8)	5	2-Pole selection	5	NA	Bank 5 , 1/2-pole selection	87
11	SWITCH(8)	6	2-Pole selection	6	NA	Bank 6 , 1/2-pole selection	93
11	SWITCH(8)	7	2-Pole selection	7	NA	Bank 7 , 1/2-pole selection	97
11	SWITCH(8)	8	2-Pole selection	8	NA	Bank 8 , 1/2-pole selection	102
12	SWITCH(8)	1	Pole shorting	1	NA	Bank 1 , 1/2-pole selection	67
12	SWITCH(8)	2	Pole shorting	2	NA	Bank 2 , 1/2-pole selection	75
12	SWITCH(8)	3	Pole shorting	3	NA	Bank 3 , 1/2-pole selection	79
12	SWITCH(8)	4	Pole shorting	4	NA	Bank 4 , 1/2-pole selection	84
12	SWITCH(8)	5	Pole shorting	5	NA	Bank 5 , 1/2-pole selection	88
12	SWITCH(8)	6	Pole shorting	6	NA	Bank 6 , 1/2-pole selection	94
12	SWITCH(8)	7	Pole shorting	7	NA	Bank 7 , 1/2-pole selection	98
12	SWITCH(8)	8	Pole shorting	8	NA	Bank 8 , 1/2-pole selection	103

TABLE 4.9 Physical Relay To Software Sub-Unit Cross Reference (continued)

Logical Sub-Unit	Sub-unit Type	Logical Chan	Switch Function	Bank	Channel	Function	Relay (RL)
13	SWITCH(8)	1	Interbank Linking	1	NA	Bank 1, interbank linking	68
13	SWITCH(8)	2	Interbank Linking	1	NA	Bank 1, interbank linking	69
13	SWITCH(8)	3	Interbank Linking	1	NA	Bank 1, interbank linking	70
13	SWITCH(8)	4	Interbank Linking	1	NA	Bank 1, interbank linking	71
13	SWITCH(8)	5	Interbank Linking	3	NA	Bank 3, interbank linking	80
13	SWITCH(8)	6	Interbank Linking	5	NA	Bank 5, interbank linking	89
13	SWITCH(8)	7	Interbank Linking	5	NA	Bank 5, interbank linking	90
13	SWITCH(8)	8	Interbank Linking	7	NA	Bank 7, interbank linking	99

Note 1:- Bank references listed above relate to an 8-bank configuration, for variants the bank identifiers will change.

TABLE 4.10 Software Sub-Unit User Channel Set-up

8 Banks 16 Channel 1-pole

Channels		Bank	Relay (RL)	Sub Unit \ Logical Channel
1	2	1	1	1 \ 1
3	4	1	2	1 \ 2
5	6	1	3	1 \ 3
7	8	1	4	1 \ 4
9	10	1	5	1 \ 5
11	12	1	6	1 \ 6
13	14	1	7	1 \ 7
15	16	1	8	1 \ 8
1	2	2	9	2 \ 1
3	4	2	10	2 \ 2
5	6	2	11	2 \ 3
7	8	2	12	2 \ 4
9	10	2	13	2 \ 5
11	12	2	14	2 \ 6
13	14	2	15	2 \ 7
15	16	2	16	2 \ 8
1	2	3	17	3 \ 1
3	4	3	18	3 \ 2
5	6	3	19	3 \ 3
7	8	3	20	3 \ 4
9	10	3	21	3 \ 5
11	12	3	22	3 \ 6
13	14	3	23	3 \ 7
15	16	3	24	3 \ 8
1	2	4	25	4 \ 1
3	4	4	26	4 \ 2
5	6	4	27	4 \ 3
7	8	4	28	4 \ 4
9	10	4	29	4 \ 5
11	12	4	30	4 \ 6
13	14	4	31	4 \ 7
15	16	4	32	4 \ 8

Channels		Bank	Relay (RL)	Sub Unit \ Logical Channel
1	2	5	33	5 \ 1
3	4	5	34	5 \ 2
5	6	5	35	5 \ 3
7	8	5	36	5 \ 4
9	10	5	37	5 \ 5
11	12	5	38	5 \ 6
13	14	5	39	5 \ 7
15	16	5	40	5 \ 8
1	2	6	41	6 \ 1
3	4	6	42	6 \ 2
5	6	6	43	6 \ 3
7	8	6	44	6 \ 4
9	10	6	45	6 \ 5
11	12	6	46	6 \ 6
13	14	6	47	6 \ 7
15	16	6	48	6 \ 8
1	2	7	49	7 \ 1
3	4	7	50	7 \ 2
5	6	7	51	7 \ 3
7	8	7	52	7 \ 4
9	10	7	53	7 \ 5
11	12	7	54	7 \ 6
13	14	7	55	7 \ 7
15	16	7	56	7 \ 8
1	2	8	57	8 \ 1
3	4	8	58	8 \ 2
5	6	8	59	8 \ 3
7	8	8	60	8 \ 4
9	10	8	61	8 \ 5
11	12	8	62	8 \ 6
13	14	8	63	8 \ 7
15	16	8	64	8 \ 8

Note - The two individual channels from a single relay in 1-pole mode are selected by using the 1/2-pole & pole shorting relays detailed in Table 4.11.

TABLE 4.10 Software Sub-Unit User Channel Set-up (continued)

8 Banks 8 Channel 2-pole

Channel	Bank	Relay (RL)	Sub Unit \ Logical Channel
1	1	1	1 \ 1
2	1	2	1 \ 2
3	1	3	1 \ 3
4	1	4	1 \ 4
5	1	5	1 \ 5
6	1	6	1 \ 6
7	1	7	1 \ 7
8	1	8	1 \ 8
1	2	9	2 \ 1
2	2	10	2 \ 2
3	2	11	2 \ 3
4	2	12	2 \ 4
5	2	13	2 \ 5
6	2	14	2 \ 6
7	2	15	2 \ 7
8	2	16	2 \ 8
1	3	17	3 \ 1
2	3	18	3 \ 2
3	3	19	3 \ 3
4	3	20	3 \ 4
5	3	21	3 \ 5
6	3	22	3 \ 6
7	3	23	3 \ 7
8	3	24	3 \ 8
1	4	25	4 \ 1
2	4	26	4 \ 2
3	4	27	4 \ 3
4	4	28	4 \ 4
5	4	29	4 \ 5
6	4	30	4 \ 6
7	4	31	4 \ 7
8	4	32	4 \ 8

Channel	Bank	Relay (RL)	Sub Unit \ Logical Channel
1	5	33	5 \ 1
2	5	34	5 \ 2
3	5	35	5 \ 3
4	5	36	5 \ 4
5	5	37	5 \ 5
6	5	38	5 \ 6
7	5	39	5 \ 7
8	5	40	5 \ 8
1	6	41	6 \ 1
2	6	42	6 \ 2
3	6	43	6 \ 3
4	6	44	6 \ 4
5	6	45	6 \ 5
6	6	46	6 \ 6
7	6	47	6 \ 7
8	6	48	6 \ 8
1	7	49	7 \ 1
2	7	50	7 \ 2
3	7	51	7 \ 3
4	7	52	7 \ 4
5	7	53	7 \ 5
6	7	54	7 \ 6
7	7	55	7 \ 7
8	7	56	7 \ 8
1	8	57	8 \ 1
2	8	58	8 \ 2
3	8	59	8 \ 3
4	8	60	8 \ 4
5	8	61	8 \ 5
6	8	62	8 \ 6
7	8	63	8 \ 7
8	8	64	8 \ 8

Note - The two individual channels from a single relay in 1-pole mode are selected by using the 1/2-pole & pole shorting relays detailed in Table 4.11.

TABLE 4.10 Software Sub-Unit User Channel Set-up (continued)

4 Banks 32 Channel 1-pole

Channels		Bank	Relay (RL)	Sub Unit \ Logical Channel
1	2	1	1	1 \ 1
3	4	1	2	1 \ 2
5	6	1	3	1 \ 3
7	8	1	4	1 \ 4
9	10	1	5	1 \ 5
11	12	1	6	1 \ 6
13	14	1	7	1 \ 7
15	16	1	8	1 \ 8
17	18	1	9	2 \ 1
19	20	1	10	2 \ 2
21	22	1	11	2 \ 3
23	24	1	12	2 \ 4
25	26	1	13	2 \ 5
27	28	1	14	2 \ 6
29	30	1	15	2 \ 7
31	32	1	16	2 \ 8
1	2	2	17	3 \ 1
3	4	2	18	3 \ 2
5	6	2	19	3 \ 3
7	8	2	20	3 \ 4
9	10	2	21	3 \ 5
11	12	2	22	3 \ 6
13	14	2	23	3 \ 7
15	16	2	24	3 \ 8
17	18	2	25	4 \ 1
19	20	2	26	4 \ 2
21	22	2	27	4 \ 3
23	24	2	28	4 \ 4
25	26	2	29	4 \ 5
27	28	2	30	4 \ 6
29	30	2	31	4 \ 7
31	32	2	32	4 \ 8

Channels		Bank	Relay (RL)	Sub Unit \ Logical Channel
1	2	3	33	5 \ 1
3	4	3	34	5 \ 2
5	6	3	35	5 \ 3
7	8	3	36	5 \ 4
9	10	3	37	5 \ 5
11	12	3	38	5 \ 6
13	14	3	39	5 \ 7
15	16	3	40	5 \ 8
17	18	3	41	6 \ 1
19	20	3	42	6 \ 2
21	22	3	43	6 \ 3
23	24	3	44	6 \ 4
25	26	3	45	6 \ 5
27	28	3	46	6 \ 6
29	30	3	47	6 \ 7
31	32	3	48	6 \ 8
1	2	4	49	7 \ 1
3	4	4	50	7 \ 2
5	6	4	51	7 \ 3
7	8	4	52	7 \ 4
9	10	4	53	7 \ 5
11	12	4	54	7 \ 6
13	14	4	55	7 \ 7
15	16	4	56	7 \ 8
17	18	4	57	8 \ 1
19	20	4	58	8 \ 2
21	22	4	59	8 \ 3
23	24	4	60	8 \ 4
25	26	4	61	8 \ 5
27	28	4	62	8 \ 6
29	30	4	63	8 \ 7
31	32	4	64	8 \ 8

Note - The two individual channels from a single relay in 1-pole mode are selected by using the 1/2-pole & pole shorting relays detailed in Table 4.11.

TABLE 4.10 Software Sub-Unit User Channel Set-up (continued)

4 Banks 16 Channel 2-pole

Channel	Bank	Relay (RL)	Sub Unit \ Logical Channel
1	1	1	1 \ 1
2	1	2	1 \ 2
3	1	3	1 \ 3
4	1	4	1 \ 4
5	1	5	1 \ 5
6	1	6	1 \ 6
7	1	7	1 \ 7
8	1	8	1 \ 8
9	1	9	2 \ 1
10	1	10	2 \ 2
11	1	11	2 \ 3
12	1	12	2 \ 4
13	1	13	2 \ 5
14	1	14	2 \ 6
15	1	15	2 \ 7
16	1	16	2 \ 8
1	2	17	3 \ 1
2	2	18	3 \ 2
3	2	19	3 \ 3
4	2	20	3 \ 4
5	2	21	3 \ 5
6	2	22	3 \ 6
7	2	23	3 \ 7
8	2	24	3 \ 8
9	2	25	4 \ 1
10	2	26	4 \ 2
11	2	27	4 \ 3
12	2	28	4 \ 4
13	2	29	4 \ 5
14	2	30	4 \ 6
15	2	31	4 \ 7
16	2	32	4 \ 8

Channel	Bank	Relay (RL)	Sub Unit \ Logical Channel
1	3	33	5 \ 1
2	3	34	5 \ 2
3	3	35	5 \ 3
4	3	36	5 \ 4
5	3	37	5 \ 5
6	3	38	5 \ 6
7	3	39	5 \ 7
8	3	40	5 \ 8
9	3	41	6 \ 1
10	3	42	6 \ 2
11	3	43	6 \ 3
12	3	44	6 \ 4
13	3	45	6 \ 5
14	3	46	6 \ 6
15	3	47	6 \ 7
16	3	48	6 \ 8
1	4	49	7 \ 1
2	4	50	7 \ 2
3	4	51	7 \ 3
4	4	52	7 \ 4
5	4	53	7 \ 5
6	4	54	7 \ 6
7	4	55	7 \ 7
8	4	56	7 \ 8
9	4	57	8 \ 1
10	4	58	8 \ 2
11	4	59	8 \ 3
12	4	60	8 \ 4
13	4	61	8 \ 5
14	4	62	8 \ 6
15	4	63	8 \ 7
16	4	64	8 \ 8

Note - The two individual channels from a single relay in 1-pole mode are selected by using the 1/2-pole & pole shorting relays detailed in Table 4.11.

TABLE 4.10 Software Sub-Unit User Channel Set-up (continued)

2 Banks 64 Channel 1-pole

Channels		Bank	Relay (RL)	Sub Unit \ Logical Channel
1	2	1	1	1 \ 1
3	4	1	2	1 \ 2
5	6	1	3	1 \ 3
7	8	1	4	1 \ 4
9	10	1	5	1 \ 5
11	12	1	6	1 \ 6
13	14	1	7	1 \ 7
15	16	1	8	1 \ 8
17	18	1	9	2 \ 1
19	20	1	10	2 \ 2
21	22	1	11	2 \ 3
23	24	1	12	2 \ 4
25	26	1	13	2 \ 5
27	28	1	14	2 \ 6
29	30	1	15	2 \ 7
31	32	1	16	2 \ 8
33	34	1	17	3 \ 1
35	36	1	18	3 \ 2
37	38	1	19	3 \ 3
39	40	1	20	3 \ 4
41	42	1	21	3 \ 5
43	44	1	22	3 \ 6
45	46	1	23	3 \ 7
47	48	1	24	3 \ 8
49	50	1	25	4 \ 1
51	52	1	26	4 \ 2
53	54	1	27	4 \ 3
55	56	1	28	4 \ 4
57	58	1	29	4 \ 5
59	60	1	30	4 \ 6
61	62	1	31	4 \ 7
63	64	1	32	4 \ 8

Channels		Bank	Relay (RL)	Sub Unit \ Logical Channel
1	2	2	33	5 \ 1
3	4	2	34	5 \ 2
5	6	2	35	5 \ 3
7	8	2	36	5 \ 4
9	10	2	37	5 \ 5
11	12	2	38	5 \ 6
13	14	2	39	5 \ 7
15	16	2	40	5 \ 8
17	18	2	41	6 \ 1
19	20	2	42	6 \ 2
21	22	2	43	6 \ 3
23	24	2	44	6 \ 4
25	26	2	45	6 \ 5
27	28	2	46	6 \ 6
29	30	2	47	6 \ 7
31	32	2	48	6 \ 8
33	34	2	49	7 \ 1
35	36	2	50	7 \ 2
37	38	2	51	7 \ 3
39	40	2	52	7 \ 4
41	42	2	53	7 \ 5
43	44	2	54	7 \ 6
45	46	2	55	7 \ 7
47	48	2	56	7 \ 8
49	50	2	57	8 \ 1
51	52	2	58	8 \ 2
53	54	2	59	8 \ 3
55	56	2	60	8 \ 4
57	58	2	61	8 \ 5
59	60	2	62	8 \ 6
61	62	2	63	8 \ 7
63	64	2	64	8 \ 8

Note - The two individual channels from a single relay in 1-pole mode are selected by using the 1/2-pole & pole shorting relays detailed in Table 4.11.

TABLE 4.10 Software Sub-Unit User Channel Set-up (continued)

2 Banks 32 Channel 2-pole

Channel	Bank	Relay (RL)	Sub Unit \ Logical Channel
1	1	1	1 \ 1
2	1	2	1 \ 2
3	1	3	1 \ 3
4	1	4	1 \ 4
5	1	5	1 \ 5
6	1	6	1 \ 6
7	1	7	1 \ 7
8	1	8	1 \ 8
9	1	9	2 \ 1
10	1	10	2 \ 2
11	1	11	2 \ 3
12	1	12	2 \ 4
13	1	13	2 \ 5
14	1	14	2 \ 6
15	1	15	2 \ 7
16	1	16	2 \ 8
17	1	17	3 \ 1
18	1	18	3 \ 2
19	1	19	3 \ 3
20	1	20	3 \ 4
21	1	21	3 \ 5
22	1	22	3 \ 6
23	1	23	3 \ 7
24	1	24	3 \ 8
25	1	25	4 \ 1
26	1	26	4 \ 2
27	1	27	4 \ 3
28	1	28	4 \ 4
29	1	29	4 \ 5
30	1	30	4 \ 6
31	1	31	4 \ 7
32	1	32	4 \ 8

Channel	Bank	Relay (RL)	Sub Unit \ Logical Channel
1	2	33	5 \ 1
2	2	34	5 \ 2
3	2	35	5 \ 3
4	2	36	5 \ 4
5	2	37	5 \ 5
6	2	38	5 \ 6
7	2	39	5 \ 7
8	2	40	5 \ 8
9	2	41	6 \ 1
10	2	42	6 \ 2
11	2	43	6 \ 3
12	2	44	6 \ 4
13	2	45	6 \ 5
14	2	46	6 \ 6
15	2	47	6 \ 7
16	2	48	6 \ 8
17	2	49	7 \ 1
18	2	50	7 \ 2
19	2	51	7 \ 3
20	2	52	7 \ 4
21	2	53	7 \ 5
22	2	54	7 \ 6
23	2	55	7 \ 7
24	2	56	7 \ 8
25	2	57	8 \ 1
26	2	58	8 \ 2
27	2	59	8 \ 3
28	2	60	8 \ 4
29	2	61	8 \ 5
30	2	62	8 \ 6
31	2	63	8 \ 7
32	2	64	8 \ 8

Note - The two individual channels from a single relay in 1-pole mode are selected by using the 1/2-pole & pole shorting relays detailed in Table 4.11.

TABLE 4.10 Software Sub-Unit User Channel Set-up (continued)

1 Bank 128 Channel 1-pole

Channels		Bank	Relay (RL)	Sub Unit \ Logical Channel
1	2	1	1	1 \ 1
3	4	1	2	1 \ 2
5	6	1	3	1 \ 3
7	8	1	4	1 \ 4
9	10	1	5	1 \ 5
11	12	1	6	1 \ 6
13	14	1	7	1 \ 7
15	16	1	8	1 \ 8
17	18	1	9	2 \ 1
19	20	1	10	2 \ 2
21	22	1	11	2 \ 3
23	24	1	12	2 \ 4
25	26	1	13	2 \ 5
27	28	1	14	2 \ 6
29	30	1	15	2 \ 7
31	32	1	16	2 \ 8
33	34	1	17	3 \ 1
35	36	1	18	3 \ 2
37	38	1	19	3 \ 3
39	40	1	20	3 \ 4
41	42	1	21	3 \ 5
43	44	1	22	3 \ 6
45	46	1	23	3 \ 7
47	48	1	24	3 \ 8
49	50	1	25	4 \ 1
51	52	1	26	4 \ 2
53	54	1	27	4 \ 3
55	56	1	28	4 \ 4
57	58	1	29	4 \ 5
59	60	1	30	4 \ 6
61	62	1	31	4 \ 7
63	64	1	32	4 \ 8

Channels		Bank	Relay (RL)	Sub Unit \ Logical Channel
65	66	1	33	5 \ 1
67	68	1	34	5 \ 2
69	70	1	35	5 \ 3
71	72	1	36	5 \ 4
73	74	1	37	5 \ 5
75	76	1	38	5 \ 6
77	78	1	39	5 \ 7
79	80	1	40	5 \ 8
81	82	1	41	6 \ 1
83	84	1	42	6 \ 2
85	86	1	43	6 \ 3
87	88	1	44	6 \ 4
89	90	1	45	6 \ 5
91	92	1	46	6 \ 6
93	94	1	47	6 \ 7
95	96	1	48	6 \ 8
97	98	1	49	7 \ 1
99	100	1	50	7 \ 2
101	102	1	51	7 \ 3
103	104	1	52	7 \ 4
105	106	1	53	7 \ 5
107	108	1	54	7 \ 6
109	110	1	55	7 \ 7
111	112	1	56	7 \ 8
113	114	1	57	8 \ 1
115	116	1	58	8 \ 2
117	118	1	59	8 \ 3
119	120	1	60	8 \ 4
121	122	1	61	8 \ 5
123	124	1	62	8 \ 6
125	126	1	63	8 \ 7
127	128	1	64	8 \ 8

Note - The two individual channels from a single relay in 1-pole mode are selected by using the 1/2-pole & pole shorting relays detailed in Table 4.11.

TABLE 4.10 Software Sub-Unit User Channel Set-up (continued)

1 Bank 64 Channel 2-pole

Channel	Bank	Relay (RL)	Sub Unit \ Logical Channel
1	1	1	1 \ 1
2	1	2	1 \ 2
3	1	3	1 \ 3
4	1	4	1 \ 4
5	1	5	1 \ 5
6	1	6	1 \ 6
7	1	7	1 \ 7
8	1	8	1 \ 8
9	1	9	2 \ 1
10	1	10	2 \ 2
11	1	11	2 \ 3
12	1	12	2 \ 4
13	1	13	2 \ 5
14	1	14	2 \ 6
15	1	15	2 \ 7
16	1	16	2 \ 8
17	1	17	3 \ 1
18	1	18	3 \ 2
19	1	19	3 \ 3
20	1	20	3 \ 4
21	1	21	3 \ 5
22	1	22	3 \ 6
23	1	23	3 \ 7
24	1	24	3 \ 8
25	1	25	4 \ 1
26	1	26	4 \ 2
27	1	27	4 \ 3
28	1	28	4 \ 4
29	1	29	4 \ 5
30	1	30	4 \ 6
31	1	31	4 \ 7
32	1	32	4 \ 8

Channel	Bank	Relay (RL)	Sub Unit \ Logical Channel
33	1	33	5 \ 1
34	1	34	5 \ 2
35	1	35	5 \ 3
36	1	36	5 \ 4
37	1	37	5 \ 5
38	1	38	5 \ 6
39	1	39	5 \ 7
40	1	40	5 \ 8
41	1	41	6 \ 1
42	1	42	6 \ 2
43	1	43	6 \ 3
44	1	44	6 \ 4
45	1	45	6 \ 5
46	1	46	6 \ 6
47	1	47	6 \ 7
48	1	48	6 \ 8
49	1	49	7 \ 1
50	1	50	7 \ 2
51	1	51	7 \ 3
52	1	52	7 \ 4
53	1	53	7 \ 5
54	1	54	7 \ 6
55	1	55	7 \ 7
56	1	56	7 \ 8
57	1	57	8 \ 1
58	1	58	8 \ 2
59	1	59	8 \ 3
60	1	60	8 \ 4
61	1	61	8 \ 5
62	1	62	8 \ 6
63	1	63	8 \ 7
64	1	64	8 \ 8

Note - The two individual channels from a single relay in 1-pole mode are selected by using the 1/2-pole & pole shorting relays detailed in Table 4.11.

TABLE 4.11 Software Sub-Unit Multiplexer Configuration Set-up

8 Banks 16 Channel 1-pole (See Note 2)				
Function	Bank	Relay (RL)	Sub Unit \ Logical Channel	Comments
1-Pole selection	1	65	10 \ 1	See Note 1
2-Pole selection	1	66	11 \ 1	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	1	67	12 \ 1	Only required when routing .2 signals to .1 front panel connector pin
Isolation	1	72	9 \ 1	
1-Pole selection	2	73	10 \ 2	See Note 1
2-Pole selection	2	74	11 \ 2	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	2	75	12 \ 2	Only required when routing .2 signals to .1 front panel connector pin
Isolation	2	76	9 \ 2	
1-Pole selection	3	77	10 \ 3	See Note 1
2-Pole selection	3	78	11 \ 3	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	3	79	12 \ 3	Only required when routing .2 signals to .1 front panel connector pin
Isolation	3	81	9 \ 3	
1-Pole selection	4	82	10 \ 4	See Note 1
2-Pole selection	4	83	11 \ 4	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	4	84	12 \ 4	Only required when routing .2 signals to .1 front panel connector pin
Isolation	4	85	9 \ 4	
1-Pole selection	5	86	10 \ 5	See Note 1
2-Pole selection	5	87	11 \ 5	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	5	88	12 \ 5	Only required when routing .2 signals to .1 front panel connector pin
Isolation	5	91	9 \ 5	
1-Pole selection	6	92	10 \ 6	See Note 1
2-Pole selection	6	93	11 \ 6	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	6	94	12 \ 6	Only required when routing .2 signals to .1 front panel connector pin
Isolation	6	95	9 \ 6	
1-Pole selection	7	96	10 \ 7	See Note 1
2-Pole selection	7	97	11 \ 7	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	7	98	12 \ 7	Only required when routing .2 signals to .1 front panel connector pin
Isolation	7	100	9 \ 7	
1-Pole selection	8	101	10 \ 8	See Note 1
2-Pole selection	8	102	11 \ 8	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	8	103	12 \ 8	Only required when routing .2 signals to .1 front panel connector pin
Isolation	8	104	9 \ 8	

Note 1:- Do NOT energise the 1-pole & 2-pole selection relays at the same time as applied channel signals will be shorted together.

Note 2:- The above 1-pole configurations assume that the .1 common pin(s) are being used on the front panel connector.

TABLE 4.11 Software Sub-Unit Multiplexer Configuration Set-up (continued)

8 Banks 8 Channel 2-pole (See Note)			
Function	Bank	Relay (RL)	Sub Unit \ Logical Channel
1-Pole selection	1	65	10 \ 1
2-Pole selection	1	66	11 \ 1
Isolation	1	72	9 \ 1
1-Pole selection	2	73	10 \ 2
2-Pole selection	2	74	11 \ 2
Isolation	2	76	9 \ 2
1-Pole selection	3	77	10 \ 3
2-Pole selection	3	78	11 \ 3
Isolation	3	81	9 \ 3
1-Pole selection	4	82	10 \ 4
2-Pole selection	4	83	11 \ 4
Isolation	4	85	9 \ 4
1-Pole selection	5	86	10 \ 5
2-Pole selection	5	87	11 \ 5
Isolation	5	91	9 \ 5
1-Pole selection	6	92	10 \ 6
2-Pole selection	6	93	11 \ 6
Isolation	6	95	9 \ 6
1-Pole selection	7	96	10 \ 7
2-Pole selection	7	97	11 \ 7
Isolation	7	100	9 \ 7
1-Pole selection	8	101	10 \ 8
2-Pole selection	8	102	11 \ 8
Isolation	8	104	9 \ 8

Note :- The above 1-pole configurations assume that the .1 common pin(s) are being used on the front panel connector.

TABLE 4.11 Software Sub-Unit Multiplexer Configuration Set-up (continued)

4 Banks 32 Channel 1-pole (See Note 2)				
Function	Bank	Relay (RL)	Sub Unit \ Logical Channel	Comments
1-Pole selection	1	65	10 \ 1	See Note 1
1-Pole selection	1	73	10 \ 2	See Note 1
2-Pole selection	1	66	11 \ 1	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
2-Pole selection	1	74	11 \ 2	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
Interbank Linking	1	68	13 \ 1	
Isolation	1	72	9 \ 1	
Pole shorting	1	67	12 \ 1	Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	1	75	12 \ 2	Only required when routing .2 signals to .1 front panel connector pin
1-Pole selection	2	77	10 \ 3	See Note 1
1-Pole selection	2	82	10 \ 4	See Note 1
2-Pole selection	2	78	11 \ 3	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
2-Pole selection	2	83	11 \ 4	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
Interbank Linking	2	80	13 \ 5	
Isolation	2	81	9 \ 3	
Pole shorting	2	79	12 \ 3	Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	2	84	12 \ 4	Only required when routing .2 signals to .1 front panel connector pin
1-Pole selection	3	86	10 \ 5	See Note 1
1-Pole selection	3	92	10 \ 6	See Note 1
2-Pole selection	3	87	11 \ 5	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
2-Pole selection	3	93	11 \ 6	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
Interbank Linking	3	89	13 \ 5	
Isolation	3	91	9 \ 5	
Pole shorting	3	88	12 \ 5	Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	3	94	12 \ 6	Only required when routing .2 signals to .1 front panel connector pin
1-Pole selection	4	96	10 \ 7	See Note 1
1-Pole selection	4	101	10 \ 8	See Note 1
2-Pole selection	4	97	11 \ 7	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
2-Pole selection	4	102	11 \ 8	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
Interbank Linking	4	99	13 \ 8	
Isolation	4	100	9 \ 7	
Pole shorting	4	98	12 \ 7	Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	4	103	12 \ 8	Only required when routing .2 signals to .1 front panel connector pin

Note 1:- Do NOT energise the 1-pole & 2-pole selection relays at the same time as applied channel signals will be shorted together.

Note 2:- The above 1-pole configurations assume that the .1 common pin(s) are being used on the front panel connector.

TABLE 4.11 Software Sub-Unit Multiplexer Configuration Set-up (continued)

4 Banks 16 Channel 2-pole (See Note)			
Function	Bank	Relay (RL)	Sub Unit \ Logical Channel
1-Pole selection	1	65	10 \ 1
1-Pole selection	1	73	10 \ 2
2-Pole selection	1	66	11 \ 1
2-Pole selection	1	74	11 \ 2
Interbank Linking	1	68	13 \ 1
Isolation	1	72	9 \ 1
1-Pole selection	2	77	10 \ 3
1-Pole selection	2	82	10 \ 4
2-Pole selection	2	78	11 \ 3
2-Pole selection	2	83	11 \ 4
Interbank Linking	2	80	13 \ 5
Isolation	2	81	9 \ 3
1-Pole selection	3	86	10 \ 5
1-Pole selection	3	92	10 \ 6
2-Pole selection	3	87	11 \ 5
2-Pole selection	3	93	11 \ 6
Interbank Linking	3	89	13 \ 5
Isolation	3	91	9 \ 5
1-Pole selection	4	96	10 \ 7
1-Pole selection	4	101	10 \ 8
2-Pole selection	4	97	11 \ 7
2-Pole selection	4	102	11 \ 8
Interbank Linking	4	99	13 \ 8
Isolation	4	100	9 \ 7

Note :- The above 1-pole configurations assume that the .1 common pin(s) are being used on the front panel connector.

TABLE 4.11 Software Sub-Unit Multiplexer Configuration Set-up (continued)

2 Banks 64 Channel 1-pole				
Function	Bank	Relay (RL)	Sub Unit \ Logical Channel	Comments
1-Pole selection	1	65	10 \ 1	See Note 1
1-Pole selection	1	73	10 \ 2	See Note 1
1-Pole selection	1	77	10 \ 3	See Note 1
1-Pole selection	1	82	10 \ 4	See Note 1
2-Pole selection	1	66	11 \ 1	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
2-Pole selection	1	74	11 \ 2	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
2-Pole selection	1	78	11 \ 3	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
2-Pole selection	1	83	11 \ 4	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	1	67	12 \ 1	Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	1	75	12 \ 2	Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	1	79	12 \ 3	Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	1	84	12 \ 4	Only required when routing .2 signals to .1 front panel connector pin
Interbank Linking	1	68	13 \ 1	
Interbank Linking	1	69	13 \ 2	
Interbank Linking	1	80	13 \ 5	
Isolation	1	72	9 \ 1	
1-Pole selection	2	86	10 \ 5	See Note 1
1-Pole selection	2	92	10 \ 6	See Note 1
1-Pole selection	2	96	10 \ 7	See Note 1
1-Pole selection	2	101	10 \ 8	See Note 1
2-Pole selection	2	87	11 \ 5	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
2-Pole selection	2	93	11 \ 6	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
2-Pole selection	2	97	11 \ 7	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
2-Pole selection	2	102	11 \ 8	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	2	88	12 \ 5	Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	2	94	12 \ 6	Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	2	98	12 \ 7	Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	2	103	12 \ 8	Only required when routing .2 signals to .1 front panel connector pin
Interbank Linking	2	89	13 \ 6	
Interbank Linking	2	90	13 \ 7	
Interbank Linking	2	99	13 \ 8	
Isolation	2	91	9 \ 5	

Note 1:- Do NOT energise the 1-pole & 2-pole selection relays at the same time as applied channel signals will be shorted together.

Note 2:- The above 1-pole configurations assume that the .1 common pin(s) are being used on the front panel connector.

TABLE 4.11 Software Sub-Unit Multiplexer Configuration Set-up (continued)

2 Banks 32 Channel 2-pole (See Note)			
Function	Bank	Relay (RL)	Sub Unit \ Logical Channel
1-Pole selection	1	65	10 \ 1
1-Pole selection	1	73	10 \ 2
1-Pole selection	1	77	10 \ 3
1-Pole selection	1	82	10 \ 4
2-Pole selection	1	66	11 \ 1
2-Pole selection	1	74	11 \ 2
2-Pole selection	1	78	11 \ 3
2-Pole selection	1	83	11 \ 4
Interbank Linking	1	68	13 \ 1
Interbank Linking	1	69	13 \ 2
Interbank Linking	1	80	13 \ 5
Isolation	1	72	9 \ 1
1-Pole selection	2	86	10 \ 5
1-Pole selection	2	92	10 \ 6
1-Pole selection	2	96	10 \ 7
1-Pole selection	2	101	10 \ 8
2-Pole selection	2	87	11 \ 5
2-Pole selection	2	93	11 \ 6
2-Pole selection	2	97	11 \ 7
2-Pole selection	2	102	11 \ 8
Interbank Linking	2	89	13 \ 6
Interbank Linking	2	90	13 \ 7
Interbank Linking	2	99	13 \ 8
Isolation	2	91	9 \ 5

Note :- The above 1-pole configurations assume that the .1 common pin(s) are being used on the front panel connector.

TABLE 4.11 Software Sub-Unit Multiplexer Configuration Set-up (continued)

1 Bank 128 Channel 1-pole				
Function	Bank	Relay (RL)	Sub Unit \ Logical Channel	Comments
1-Pole selection	1	65	10 \ 1	See Note 1
1-Pole selection	1	73	10 \ 2	See Note 1
1-Pole selection	1	77	10 \ 3	See Note 1
1-Pole selection	1	82	10 \ 4	See Note 1
1-Pole selection	1	86	10 \ 5	See Note 1
1-Pole selection	1	92	10 \ 6	See Note 1
1-Pole selection	1	96	10 \ 7	See Note 1
1-Pole selection	1	101	10 \ 8	See Note 1
2-Pole selection	1	66	11 \ 1	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
2-Pole selection	1	74	11 \ 2	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
2-Pole selection	1	78	11 \ 3	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
2-Pole selection	1	83	11 \ 4	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
2-Pole selection	1	87	11 \ 5	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
2-Pole selection	1	93	11 \ 6	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
2-Pole selection	1	97	11 \ 7	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
2-Pole selection	1	102	11 \ 8	See Note 1. Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	1	67	12 \ 1	Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	1	75	12 \ 2	Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	1	79	12 \ 3	Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	1	84	12 \ 4	Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	1	88	12 \ 5	Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	1	94	12 \ 6	Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	1	98	12 \ 7	Only required when routing .2 signals to .1 front panel connector pin
Pole shorting	1	103	12 \ 8	Only required when routing .2 signals to .1 front panel connector pin
Interbank Linking	1	68	13 \ 1	
Interbank Linking	1	69	13 \ 2	
Interbank Linking	1	70	13 \ 3	
Interbank Linking	1	71	13 \ 4	
Interbank Linking	1	80	13 \ 5	
Interbank Linking	1	89	13 \ 6	
Interbank Linking	1	90	13 \ 7	
Interbank Linking	1	99	13 \ 8	
Isolation	1	72	9 \ 1	

Note 1:- Do NOT energise the 1-pole & 2-pole selection relays at the same time as applied channel signals will be shorted together.

Note 2:- The above 1-pole configurations assume that the .1 common pin(s) are being used on the front panel connector.

TABLE 4.11 Software Sub-Unit Multiplexer Configuration Set-up (continued)

1 Bank 64 Channel 2-pole (See Note)			
Function	Bank	Relay (RL)	Sub Unit \ Logical Channel
1-Pole selection	1	65	10 \ 1
1-Pole selection	1	73	10 \ 2
1-Pole selection	1	77	10 \ 3
1-Pole selection	1	82	10 \ 4
1-Pole selection	1	86	10 \ 5
1-Pole selection	1	92	10 \ 6
1-Pole selection	1	96	10 \ 7
1-Pole selection	1	101	10 \ 8
2-Pole selection	1	66	11 \ 1
2-Pole selection	1	74	11 \ 2
2-Pole selection	1	78	11 \ 3
2-Pole selection	1	83	11 \ 4
2-Pole selection	1	87	11 \ 5
2-Pole selection	1	93	11 \ 6
2-Pole selection	1	97	11 \ 7
2-Pole selection	1	102	11 \ 8
Interbank Linking	1	68	13 \ 1
Interbank Linking	1	69	13 \ 2
Interbank Linking	1	70	13 \ 3
Interbank Linking	1	71	13 \ 4
Interbank Linking	1	80	13 \ 5
Interbank Linking	1	89	13 \ 6
Interbank Linking	1	90	13 \ 7
Interbank Linking	1	99	13 \ 8
Isolation	1	72	9 \ 1

Note :- The above 1-pole configurations assume that the .1 common pin(s) are being used on the front panel connector.

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SECTION 5 - CONNECTOR PIN OUTS

Figures 5.1 to 5.9 provide pin outs for the Multiplexer Module 40-612.

	A	B	C	D	E
32	1.1	3.1	5.1	7.1	C1.1
31	1.2	3.2	5.2	7.2	C1.2
30	2.1	4.1	6.1	8.1	NC
29	2.2	4.2	6.2	8.2	NC
28	9.1	11.1	13.1	15.1	C2.1
27	9.2	11.2	13.2	15.2	C2.2
26	10.1	12.1	14.1	16.1	NC
25	10.2	12.2	14.2	16.2	NC
24	17.1	19.1	21.1	23.1	C3.1
23	17.2	19.2	21.2	23.2	C3.2
22	18.1	20.1	22.1	24.1	NC
21	18.2	20.2	22.2	24.2	NC
20	25.1	27.1	29.1	31.1	C4.1
19	25.2	27.2	29.2	31.2	C4.2
18	26.1	28.1	30.1	32.1	NC
17	26.2	28.2	30.2	32.2	NC
16	33.1	35.1	37.1	39.1	C5.1
15	33.2	35.2	37.2	39.2	C5.2
14	34.1	36.1	38.1	40.1	NC
13	34.2	36.2	38.2	40.2	NC
12	41.1	43.1	45.1	47.1	C6.1
11	41.2	43.2	45.2	47.2	C6.2
10	42.1	44.1	46.1	48.1	NC
9	42.2	44.2	46.2	48.2	NC
8	49.1	51.1	53.1	55.1	C7.1
7	49.2	51.2	53.2	55.2	C7.2
6	50.1	52.1	54.1	56.1	NC
5	50.2	52.2	54.2	56.2	NC
4	57.1	59.1	61.1	63.1	C8.1
3	57.2	59.2	61.2	63.2	C8.2
2	58.1	60.1	62.1	64.1	NC
1	58.2	60.2	62.2	64.2	GND

Figure 5.1 - Multiplexer Module 40-612: General Pin Outs

	A	B	C	D	E
32	101	105	109	113	C1
31	102	106	110	114	NC
30	103	107	111	115	NC
29	104	108	112	116	NC
28	201	205	209	213	C2
27	202	206	210	214	NC
26	203	207	211	215	NC
25	204	208	212	216	NC
24	301	305	309	313	C3
23	302	306	310	314	NC
22	303	307	311	315	NC
21	304	308	312	316	NC
20	401	405	409	413	C4
19	402	406	410	414	NC
18	403	407	411	415	NC
17	404	408	412	416	NC
16	501	505	509	513	C5
15	502	506	510	514	NC
14	503	507	511	515	NC
13	504	508	512	516	NC
12	601	605	609	613	C6
11	602	606	610	614	NC
10	603	607	611	615	NC
9	604	608	612	616	NC
8	701	705	709	713	C7
7	702	706	710	714	NC
6	703	707	711	715	NC
5	704	708	712	716	NC
4	801	805	809	813	C8
3	802	806	810	814	NC
2	803	807	811	815	NC
1	804	808	812	816	GND

Figure 5.2 - Multiplexer Module 40-612: 8 Bank, 16 Channel 1-Pole Pinout

	A	B	C	D	E
32	101.1	103.1	105.1	107.1	C1.1
31	101.2	103.2	105.2	107.2	C1.2
30	102.1	104.1	106.1	108.1	NC
29	102.2	104.2	106.2	108.2	NC
28	201.1	203.1	205.1	207.1	C2.1
27	201.2	203.2	205.2	207.2	C2.2
26	202.1	204.1	206.1	208.1	NC
25	202.2	204.2	206.2	208.2	NC
24	301.1	303.1	305.1	307.1	C3.1
23	301.2	303.2	305.2	307.2	C3.2
22	302.1	304.1	306.1	308.1	NC
21	302.2	304.2	306.2	308.2	NC
20	401.1	403.1	405.1	407.1	C4.1
19	401.2	403.2	405.2	407.2	C4.2
18	402.1	404.1	406.1	408.1	NC
17	402.2	404.2	406.2	408.2	NC
16	501.1	503.1	505.1	507.1	C5.1
15	501.2	503.2	505.2	507.2	C5.2
14	502.1	504.1	506.1	508.1	NC
13	502.2	504.2	506.2	508.2	NC
12	601.1	603.1	605.1	607.1	C6.1
11	601.2	603.2	605.2	607.2	C6.2
10	602.1	604.1	606.1	608.1	NC
9	602.2	604.2	606.2	608.2	NC
8	701.1	703.1	705.1	707.1	C7.1
7	701.2	703.2	705.2	707.2	C7.2
6	702.1	704.1	706.1	708.1	NC
5	702.2	704.2	706.2	708.2	NC
4	801.1	803.1	805.1	807.1	C8.1
3	801.2	803.2	805.2	807.2	C8.2
2	802.1	804.1	806.1	808.1	NC
1	802.2	804.2	806.2	808.2	GND

Figure 5.3 - Multiplexer Module 40-612: 8 Bank, 8 Channel 2-Pole Pinout

	A	B	C	D	E
32	101	105	109	113	C1
31	102	106	110	114	NC
30	103	107	111	115	NC
29	104	108	112	116	NC
28	117	121	125	129	NC
27	118	122	126	130	NC
26	119	123	127	131	NC
25	120	124	128	132	NC
24	201	205	209	213	C2
23	202	206	210	214	NC
22	203	207	211	215	NC
21	204	208	212	216	NC
20	217	221	225	229	NC
19	218	222	226	230	NC
18	219	223	227	231	NC
17	220	224	228	232	NC
16	301	305	309	313	C3
15	302	306	310	314	NC
14	303	307	311	315	NC
13	304	308	312	316	NC
12	317	321	325	329	NC
11	318	322	326	330	NC
10	319	323	327	331	NC
9	320	324	328	332	NC
8	401	405	409	413	C4
7	402	406	410	414	NC
6	403	407	411	415	NC
5	404	408	412	416	NC
4	417	421	425	429	NC
3	418	422	426	430	NC
2	419	423	427	431	NC
1	420	424	428	432	GND

Figure 5.4 - Multiplexer Module 40-612: 4 Bank, 32 Channel 1-Pole Pinout

	A	B	C	D	E
32	101.1	103.1	105.1	107.1	C1.1
31	101.2	103.2	105.2	107.2	C1.2
30	102.1	104.1	106.1	108.1	NC
29	102.2	104.2	106.2	108.2	NC
28	109.1	111.1	113.1	115.1	NC
27	109.2	111.2	113.2	115.2	NC
26	110.1	112.1	114.1	116.1	NC
25	110.2	112.2	114.2	116.2	NC
24	201.1	203.1	205.1	207.1	C2.1
23	201.2	203.2	205.2	207.2	C2.2
22	202.1	204.1	206.1	208.1	NC
21	202.2	204.2	206.2	208.2	NC
20	209.1	211.1	213.1	215.1	NC
19	209.2	211.2	213.2	215.2	NC
18	210.1	212.1	214.1	216.1	NC
17	210.2	212.2	214.2	216.2	NC
16	301.1	303.1	305.1	307.1	C3.1
15	301.2	303.2	305.2	307.2	C3.2
14	302.1	304.1	306.1	308.1	NC
13	302.2	304.2	306.2	308.2	NC
12	309.1	311.1	313.1	315.1	NC
11	309.2	311.2	313.2	315.2	NC
10	310.1	312.1	314.1	316.1	NC
9	310.2	312.2	314.2	316.2	NC
8	401.1	403.1	405.1	407.1	C4.1
7	401.2	403.2	405.2	407.2	C4.2
6	402.1	404.1	406.1	408.1	NC
5	402.2	404.2	406.2	408.2	NC
4	409.1	411.1	413.1	415.1	NC
3	409.2	411.2	413.2	415.2	NC
2	410.1	412.1	414.1	416.1	NC
1	410.2	412.2	414.2	416.2	GND

Figure 5.5 - Multiplexer Module 40-612: 4 Bank, 16 Channel 2-Pole Pinout

	A	B	C	D	E
32	101	105	109	113	C1
31	102	106	110	114	NC
30	103	107	111	115	NC
29	104	108	112	116	NC
28	117	121	125	129	NC
27	118	122	126	130	NC
26	119	123	127	131	NC
25	120	124	128	132	NC
24	133	137	141	145	NC
23	134	138	142	146	NC
22	135	139	143	147	NC
21	136	140	144	148	NC
20	149	153	157	161	NC
19	150	154	158	162	NC
18	151	155	159	163	NC
17	152	156	160	164	NC
16	201	205	209	213	C2
15	202	206	210	214	NC
14	203	207	211	215	NC
13	204	208	212	216	NC
12	217	221	225	229	NC
11	218	222	226	230	NC
10	219	223	227	231	NC
9	220	224	228	232	NC
8	233	237	241	245	NC
7	234	238	242	246	NC
6	235	239	243	247	NC
5	236	240	244	248	NC
4	249	253	257	261	NC
3	250	254	258	262	NC
2	251	255	259	263	NC
1	252	256	260	264	GND

Figure 5.6 - Multiplexer Module 40-612: 2 Bank, 64 Channel 1-Pole Pinout

	A	B	C	D	E
32	101.1	103.1	105.1	107.1	C1.1
31	101.2	103.2	105.2	107.2	C1.2
30	102.1	104.1	106.1	108.1	NC
29	102.2	104.2	106.2	108.2	NC
28	109.1	111.1	113.1	115.1	NC
27	109.2	111.2	113.2	115.2	NC
26	110.1	112.1	114.1	116.1	NC
25	110.2	112.2	114.2	116.2	NC
24	117.1	119.1	121.1	123.1	NC
23	117.2	119.2	121.2	123.2	NC
22	118.1	120.1	122.1	124.1	NC
21	118.2	120.2	122.2	124.2	NC
20	125.1	127.1	129.1	131.1	NC
19	125.2	127.2	129.2	131.2	NC
18	126.1	128.1	130.1	132.1	NC
17	126.2	128.2	130.2	132.2	NC
16	201.1	203.1	205.1	207.1	C2.1
15	201.2	203.2	205.2	207.2	C2.2
14	202.1	204.1	206.1	208.1	NC
13	202.2	204.2	206.2	208.2	NC
12	209.1	211.1	213.1	215.1	NC
11	209.2	211.2	213.2	215.2	NC
10	210.1	212.1	214.1	216.1	NC
9	210.2	212.2	214.2	216.2	NC
8	217.1	219.1	221.1	223.1	NC
7	217.2	219.2	221.2	223.2	NC
6	218.1	220.1	222.1	224.1	NC
5	218.2	220.2	222.2	224.2	NC
4	225.1	227.1	229.1	231.1	NC
3	225.2	227.2	229.2	231.2	NC
2	226.1	228.1	230.1	232.1	NC
1	226.2	228.2	230.2	232.2	GND

Figure 5.7 - Multiplexer Module 40-612: 2 Bank, 32 Channel 2-Pole Pinout

	A	B	C	D	E
32	1	5	9	13	C1
31	2	6	10	14	NC
30	3	7	11	15	NC
29	4	8	12	16	NC
28	17	21	25	29	NC
27	18	22	26	30	NC
26	19	23	27	31	NC
25	20	24	28	32	NC
24	33	37	41	45	NC
23	34	38	42	46	NC
22	35	39	43	47	NC
21	36	40	44	48	NC
20	49	53	57	61	NC
19	50	54	58	62	NC
18	51	55	59	63	NC
17	52	56	60	64	NC
16	65	69	73	77	NC
15	66	70	74	78	NC
14	67	71	75	79	NC
13	68	72	76	80	NC
12	81	85	89	93	NC
11	82	86	90	94	NC
10	83	87	91	95	NC
9	84	88	92	96	NC
8	97	101	105	109	NC
7	98	102	106	110	NC
6	99	103	107	111	NC
5	100	104	108	112	NC
4	113	117	121	125	NC
3	114	118	122	126	NC
2	115	119	123	127	NC
1	116	120	124	128	GND

Figure 5.8 - Multiplexer Module 40-612: 1 Bank, 128 Channel 1-Pole Pinout

	A	B	C	D	E
32	101.1	103.1	105.1	107.1	C1.1
31	101.2	103.2	105.2	107.2	C1.2
30	102.1	104.1	106.1	108.1	NC
29	102.2	104.2	106.2	108.2	NC
28	109.1	111.1	113.1	115.1	NC
27	109.2	111.2	113.2	115.2	NC
26	110.1	112.1	114.1	116.1	NC
25	110.2	112.2	114.2	116.2	NC
24	117.1	119.1	121.1	123.1	NC
23	117.2	119.2	121.2	123.2	NC
22	118.1	120.1	122.1	124.1	NC
21	118.2	120.2	122.2	124.2	NC
20	125.1	127.1	129.1	131.1	NC
19	125.2	127.2	129.2	131.2	NC
18	126.1	128.1	130.1	132.1	NC
17	126.2	128.2	130.2	132.2	NC
16	133.1	135.1	137.1	139.1	NC
15	133.2	135.2	137.2	139.2	NC
14	134.1	136.1	138.1	140.1	NC
13	134.2	136.2	138.2	140.2	NC
12	141.1	143.1	145.1	147.1	NC
11	141.2	143.2	145.2	147.2	NC
10	142.1	144.1	146.1	148.1	NC
9	142.2	144.2	146.2	148.2	NC
8	149.1	151.1	153.1	155.1	NC
7	149.2	151.2	153.2	155.2	NC
6	150.1	152.1	154.1	156.1	NC
5	150.2	152.2	154.2	156.2	NC
4	157.1	159.1	161.1	163.1	NC
3	157.2	159.2	161.2	163.2	NC
2	158.1	160.1	162.1	164.1	NC
1	158.2	160.2	162.2	164.2	GND

Figure 5.8 - Multiplexer Module 40-612: 1 Bank, 64 Channel 2-Pole Pinout

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SECTION 6 - TROUBLESHOOTING

INSTALLATION PROBLEMS

The Plug & Play functionality of Pickering switch cards generally ensures trouble-free installation.

If you do experience any installation problems you should first ensure that all cards are properly seated in their slots. Improperly mated cards may go undetected by the operating system, or may be detected as a card of an unknown type. They can also cause the computer to freeze at various stages in the boot sequence.

If your system employs MXI-3 you should check the integrity of all MXI-3 links. When the system is powered up, and during Windows start-up, you should expect to see periodic activity on the MXI-3 RX/TX (yellow) indicators, clearing to leave only the PWR/LNK (green) LEDs illuminated. The RX/TX indicators should show activity when you attempt to access a card.

DIAGNOSTIC UTILITY

The Pickering Diagnostic Utility (accessible through the Programs>>Pickering>>PXI Utilities menu) generates a diagnostic report of the system's PCI configuration, highlighting any potential configuration problems. Specific details of all installed Pickering switch cards are included. All the installed Pickering switch cards should be listed in the "Pilpxi information" section - if one or more cards is missing it may be possible to determine the reason by referring to the PCI configuration dump contained in the report, but interpretation of this information is far from straightforward, and the best course is to contact Pickering support: support@pickeringtest.com, if possible including a copy of the diagnostic report.

In the "VISA information" section, if VISA is not installed it's absence will be reported. This does not affect operation using the Direct I/O driver, and is not a problem unless you wish to use VISA. VISA is a component of National Instruments LabWindows/CVI and LabVIEW, or is available as a standalone environment.

If VISA is present and is of a sufficiently recent version, the section "Pipx40 information" should present a listing similar to "Pilpxi information".

Please note that the Diagnostic Utility cannot access cards if they are currently opened by some other application, such as the Test Panels or Terminal Monitor.

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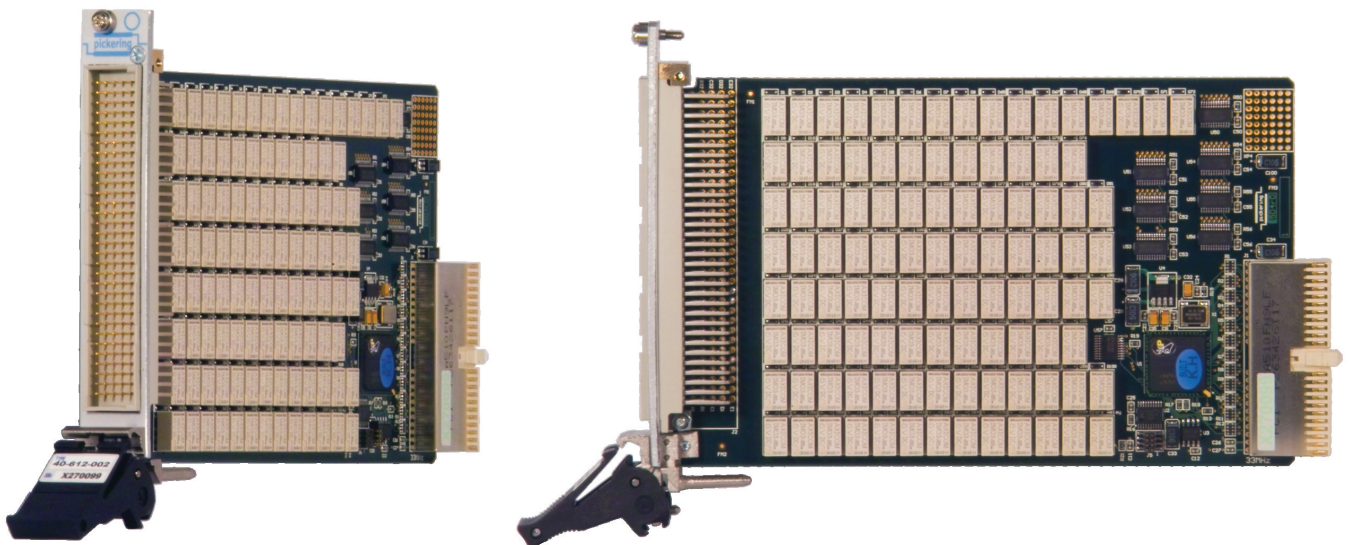
SECTION 7 - FUNCTIONAL DESCRIPTION

MECHANICAL DESCRIPTION

The Multiplexer Module 40-612 conforms to the 3U height (128mm) Eurocard standard. The module comprises the following:

- CPCI Ejector Handle
- Front Panel mounted 160-way DIN41612 connector
- 105 Electro-mechanical signal relays
- Compact PCI backplane connector
- FPGA (U1)
- Control Logic

The front panel is secured to the PCB by two M2.5 x 6mm pan-head posi-drive screws.



FUNCTIONAL DESCRIPTION

A functional block diagram is provided in Figure 7.1. The Module is powered by 5V and +3.3V inputs via Compact PCI connector J1. The interface to the user test equipment is via the front panel mounted 160-way DIN41612 connector, J2. The module comprises a PCB populated with 105 Electro-Mechanical relays configured as eight separate 8 channel multiplexers, with two pole switching. The relays are energised via control signals from relay drivers U50 to U56. The relay drivers are addressed by FPGA U1 to output the required signal.

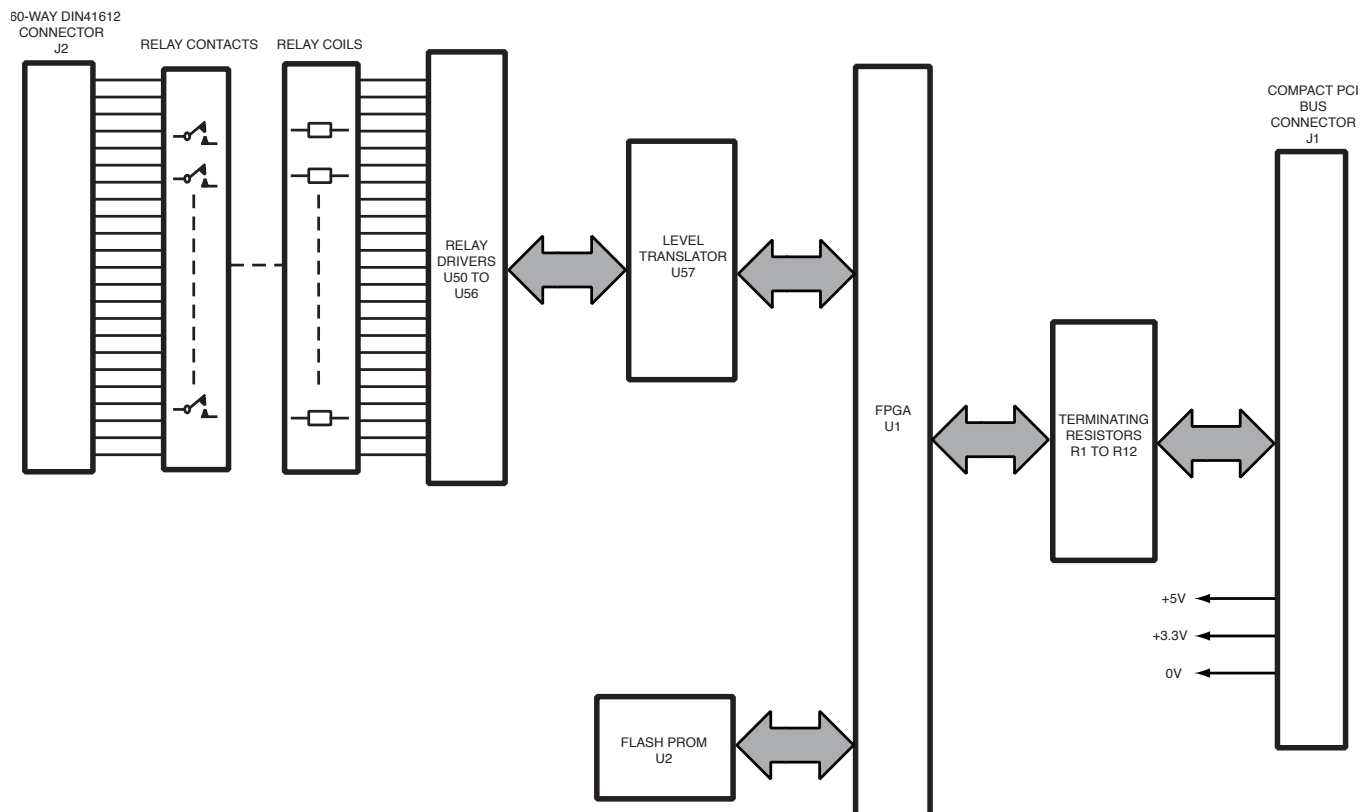


Figure 7.1 - Very High Density Versatile Multiplexer Module 40-612: Functional Block Diagram

SECTION 8 - PARTS LIST

The following pages provide parts lists and a component layout diagram for Very High Density Versatile Multiplexer Module 40-612.

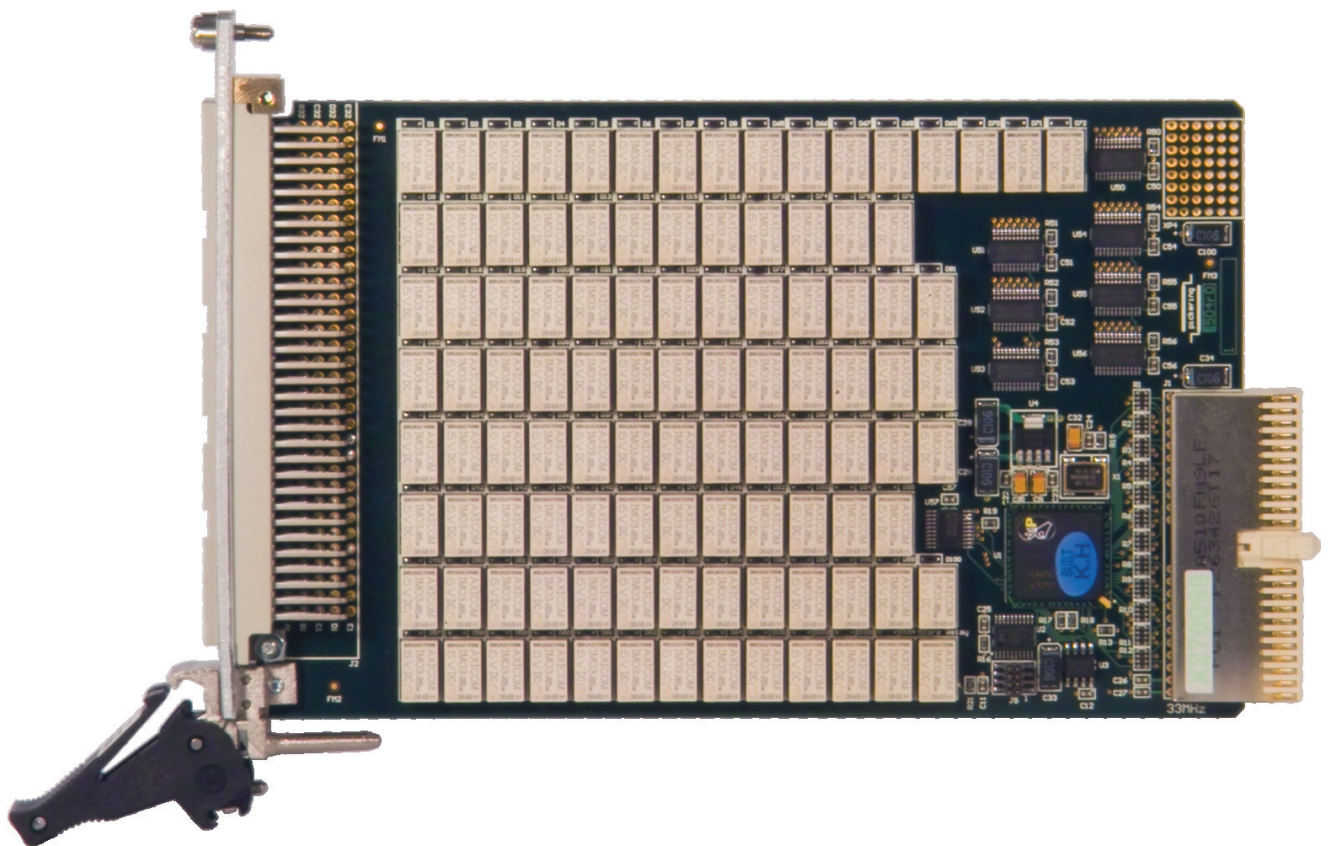


Table 8.1 provides a parts list and Figures 8.1 and 8.2 component layout diagrams for the 40-612 Multiplexer Module.

TABLE 8.1 - Very High Density Versatile Multiplexer Module 40-612 Parts List

Circuit Reference	Description	Value / Type	Part Number	Qty
R1-12	Resistor Network (4 res, 8 pins)	10R	C/RS/102	12
R13-15	Resistor (1/16W, 1%)	10R	C/RS/529	3
R16	Resistor (1/16W, 1%)	3K3	C/RS/495	1
R17	Resistor (1/16W, 1%)	2K4	C/RS/540	1
R18	Resistor (1/16W, 1%)	4K7	C/RS/146	1
R19	Resistor (1/16W, 1%)	1K	C/RS/148	1
R21	Resistor (1/16W, 1%)	100R	C/RS/147	1
R50-56	Resistor (1/16W, 1%)	590R	C/RS/447	7
C1-27, 50-57	Capacitor, Ceramic	100nF	C/CP/034	35
C28, 29, 33, 34, 100	Capacitor, Tantalum	10uF, 16V	C/CP/024	5
C30-32	Capacitor, Tantalum	10uF, 10V	C/CP/051	3
D1-104	Diode, Small Signal	1SS355TE-17C	C/SC/056	104
U1	IC, FPGA (Xilinx Spartan-II)	XC2S200-5FG256C	C/IC/210	1
U2	IC, Flash PROM (Xilinx XCF00S Series)	XCF02SV020C	C/IC/183	1
U3	IC, Serial EEPROM	M93CS86-MN6	C/IC/113	1
U4	IC, Voltage Regulator (+2.5V, Low Dropout)	LP3961EMP-2.5	C/IC/159	1
U50-56	IC, LED driver	MBI5026CP	C/IC/124	7
U57	IC, Bi-directional Transceiver	MM74HCT245MTCX	C/IC/185	1
X1	Crystal, 25MHz	SPX0018541 (CMAC)	C/MS/232	1
J1	Connector, PCB mount (right angle) female	150-pins (6 x 25-way)	C/CN/355	1
For J1	Connector coding key	"brilliant blue"	C/MS/071	1
J2	Connector, PCB mount (right angle) male	160-way	C/CN/734	1
J5	Connector, PCB mount (straight) male	2 x 4-way	C/CN/683	1
XP4	Connector, PCB mount (right angle) female	48-pins (6 x 8-way)	NOT FITTED	1
RL1-105	Relay, Electro-mech (DPCO, 2 form C)	DPDT	C/RL/199	105

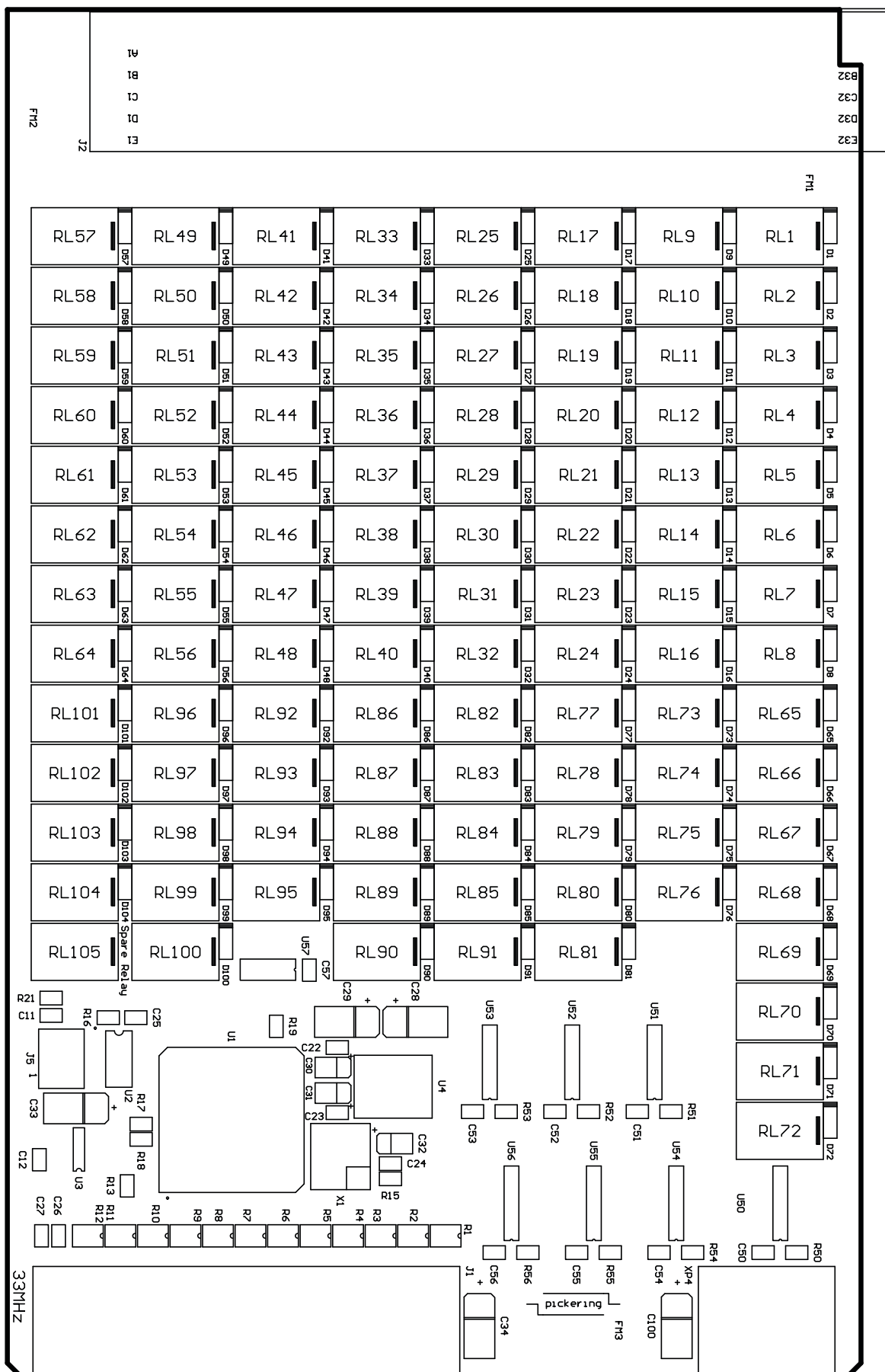


Figure 8.1 - Very High Density Versatile Multiplexer Module 40-612: Component Layout

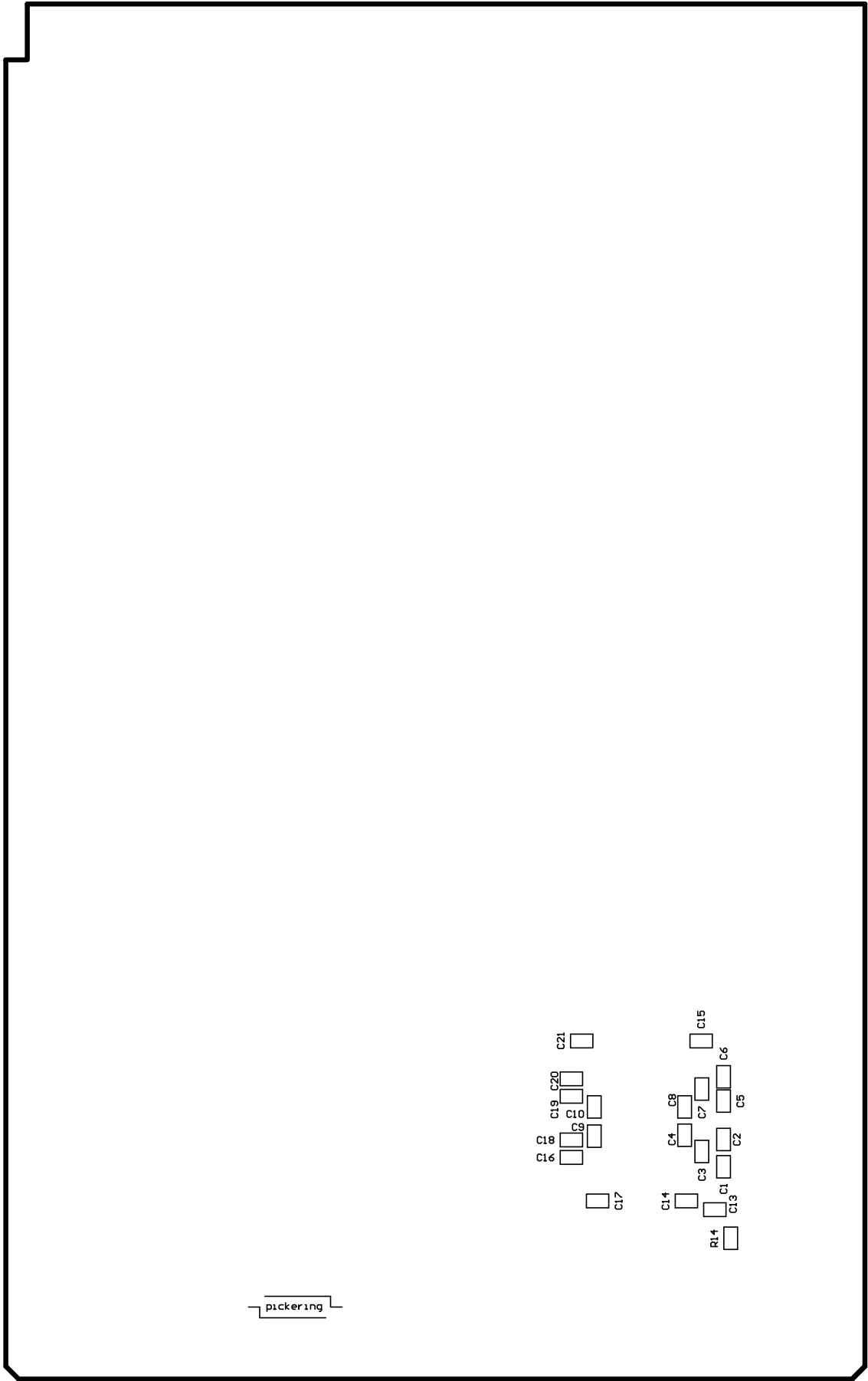


Figure 8.2 - Very High Density Versatile Multiplexer Module 40-612: Component Layout

SECTION 9 - CAUTION



CAUTION

Handling of Electrostatic-Sensitive Semiconductor Devices

Certain semiconductor devices used in the equipment are liable to damage due to static voltage. Observe the following precautions when handling these devices in their unterminated state, or sub-units containing these devices:

- (1) Persons removing sub-units from an equipment using these devices must be earthed by a wrist strap and a resistor at the point provided on the equipment.
- (2) Soldering irons used during the repair operations must be low voltage types with earthed tips and isolated from the mains voltage by a double insulated transformer.
- (3) Outer clothing worn must be unable to generate static charges.
- (4) Printed Circuit Boards (PCBs) fitted with these devices must be stored and transported in anti-static bags.

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